SBAS422A – JULY 2007 – REVISED SEPTEMBER 2007

16-Bit, Single-Channel, Low-Noise, Voltage-Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy: ±0.5 LSB**
- **16-Bit Monotonic Over Temperature Range**
- **Low-Noise: 24nV/√Hz**
- **Fast Settling: 5µs**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Wide, Single Power Supply: +2.7V to +5.5V**
- **DAC Loading Control**
- **Selectable Power-On Reset to Zero-Scale or Midscale**
- **Power-Down Mode**
- **Unipolar Straight Binary or 2's Complement Input Mode**
- **Fast SPI™ Interface with Schmitt-Triggered Inputs: Up To 50MHz, 1.8V/3V/5V Logic**
- **Small Package: QFN-24, 4x4mm**

APPLICATIONS

- **Industrial Process Control**
- **Data Acquisition Systems**
- **Automatic Test Equipment**
- **Communications**
- **Optical Networking**

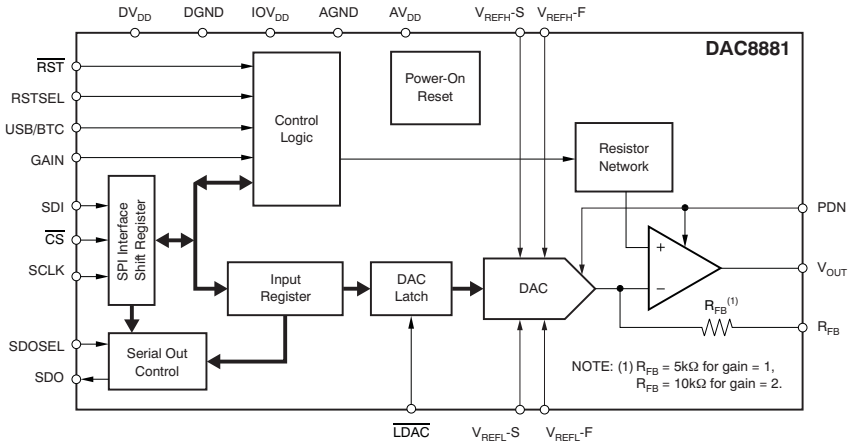
DESCRIPTION

The DAC8881 is a 16-bit, single-channel, voltage-output digital-to-analog converter (DAC) that offers low-power operation and a flexible SPI serial interface. It also features 16-bit monotonicity, excellent linearity, and fast settling time. The on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the full supply range of 2.7V to 5.5V.

The device supports a standard SPI serial interface capable of operating with input data clock frequencies up to 50MHz. The DAC8881 requires an external reference voltage to set the output range of the DAC channel. A programmable power-on reset circuit is also incorporated into the device to ensure that the DAC output powers up at zero-scale or midscale, and remains there until a valid write command.

Additionally, the device has the capability to function in either unipolar straight binary or 2's complement mode. The DAC8881 provides a power-down feature, accessed over the PDN pin, that reduces the current consumption to 25µA at 5V. Power consumption is 6mW at 5V, reducing to 125µW in power-down mode.

The DAC8881 is available in a 4x4mm QFN-24 package with a specified operating temperature range of –40°C to +105°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8881	QFN-24	RGE	–40°C to +105°C	DAC8881

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		DAC8881	UNIT
AV_{DD} to AGND		–0.3 to 6	V
DV_{DD} to DGND		–0.3 to 6	V
IOV_{DD} to DGND		–0.3 to 6	V
Digital input voltage to DGND		–0.3 to IOV_{DD} + 0.3	V
V_{OUT} to AGND		–0.3 to AV_{DD} + 0.3	V
Operating temperature range		–40 to +105	°C
Storage temperature range		–65 to +150	°C
Maximum junction temperature (T_J max)		+150	°C
ESD ratings	Human body model (HBM)	3000	V
	Charged device model (CDM)	1000	V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD}$ = +2.7V to +5.5V, IOV_{DD} = +1.8V to +5.5V, gain = 1X mode, unless otherwise noted.

PARAMETER	CONDITIONS		DAC8881 MIN	DAC8881 TYP	DAC8881 MAX	UNIT
ACCURACY						
Linearity error	Measured by line passing through codes 0200h and FE00h			±0.5	±1	LSB
Differential linearity error	Measured by line passing through codes 0200h and FE00h			±0.25	±1	LSB
Monotonicity			16			Bits
Zero-scale error	T_A = +25°C, code = 0200h				±4	LSB
	T_{MIN} to T_{MAX}, code = 0200h				±8	LSB
Zero-scale drift	Code = 0200h			±0.5	±1	ppm/°C of FSR
Gain error	T_A = +25°C, Measured by line passing through codes 0200h and FE00h			±4	±8	LSB
Gain temperature drift	Measured by line passing through codes 0200h and FE00h			±0.5	±1	ppm/°C
PSRR	V_{OUT} = full-scale, AV_{DD} = +5V ±10%				2	LSB/V
ANALOG OUTPUT(1)						
Voltage output(2)			0		AV_{DD}	V
Output voltage drift vs time	Device operating for 500 hours			5		ppm of FSR
	Device operating for 1000 hours			8		ppm of FSR
Output current				2.5		mA
Maximum load capacitance				200		pF
Short-circuit current				+31, –50		mA
REFERENCE INPUT(1)						
V_{REFH} input voltage range	AV_{DD} = +5.5V		1.25	5.0	AV_{DD}	V
	AV_{DD} = +3V		1.25	2.5	AV_{DD}	V
V_{REFH} input capacitance				5		pF
V_{REFH} input impedance				4.5		kΩ
V_{REFL} input voltage range			–0.2	0	+0.2	V
V_{REFL} input capacitance				4.5		pF
V_{REFL} input impedance				5		kΩ
DYNAMIC PERFORMANCE(1)						
Settling time	To ±0.003% FS, R_L = 10kΩ, C_L = 50pF, code 1000h to F000h			5		µs
Slew rate	From 10% to 90% of 0V to +5V			2.5		V/µs
Code change glitch	Code = 7FFFh to 8000h to 7FFFh	V_{REFH} = 5V, gain = 1X mode		37		nV-s
		V_{REFH} = 2.5V, gain = 1X mode		18		nV-s
		V_{REFH} = 1.25V, gain = 1X mode		9		nV-s
		V_{REFH} = 2.5V, gain = 2X mode		21		nV-s
		V_{REFH} = 1.25V, gain = 2X mode		10		nV-s
Digital feedthrough				1		nV-s
Output noise voltage density	f = 1kHz to 100kHz, full-scale output	Gain = 1		24	30	nV/√Hz
		Gain = 2		40	48	nV/√Hz
Output noise voltage	f = 0.1Hz to 10Hz, full-scale output			2		$µV_{PP}$

(1) Ensured by design. Not production tested.
(2) The output from the V_{OUT} pin = $[(V_{REFH} – V_{REFL})/65536] \times CODE \times$ Buffer GAIN + V_{REFL}. The maximum range of V_{OUT} is 0V to AV_{DD}. The full-scale of the output must be less than AV_{DD}; otherwise, output saturation occurs.

ELECTRICAL CHARACTERISTICS (continued)

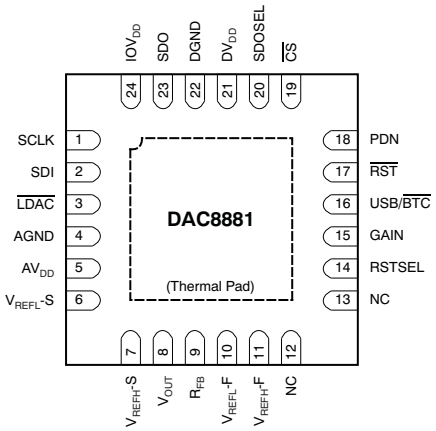
All specifications at $T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD}$ = +2.7V to +5.5V, IOV_{DD} = +1.8V to +5.5V, gain = 1X mode, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8881			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS(3)					
High-level input voltage, V_{IH}	IOV_{DD} = 4.5V to 5.5V	3.8		IOV_{DD} + 0.3	V
	IOV_{DD} = 2.7V to 3.3V	2.1		IOV_{DD} + 0.3	V
	IOV_{DD} = 1.7V to 2.0V	1.5		IOV_{DD} + 0.3	V
Low-level input voltage, V_{IL}	IOV_{DD} = 4.5V to 5.5V	–0.3		0.8	V
	IOV_{DD} = 2.7V to 3.3V	–0.3		0.6	V
	IOV_{DD} = 1.7V to 2.0V	–0.3		0.3	V
Digital input current (I_{IN})			±1	±10	µA
Digital input capacitance			5		pF
DIGITAL OUTPUT(3)					
High-level output voltage, V_{OH}	IOV_{DD} = 2.7V to 5.5V, I_{OH} = –1mA	IOV_{DD} – 0.2			V
	IOV_{DD} = 1.7V to 2.0V, I_{OH} = –500µA	IOV_{DD} – 0.2			V
Low-level output voltage, V_{OL}	IOV_{DD} = 2.7V to 5.5V, I_{OL} = 1mA			0.2	V
	IOV_{DD} = 1.7 to 2.0V, I_{OL} = 500µA			0.2	V
POWER SUPPLY					
AV_{DD}		+2.7		+5.5	V
DV_{DD}		+2.7		+5.5	V
IOV_{DD}		+1.7		DV_{DD}	V
AI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND			1.5	mA
DI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND		1	10	µA
IOI_{DD}	$V_{IH} = IOV_{DD}$, V_{IL} = DGND		1	10	µA
AI_{DD} power-down	PDN = IOV_{DD}		25	50	µA
Power dissipation	$AV_{DD} = DV_{DD}$ = 5.0V		6	7.5	mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

(3) Ensured by design. Not production tested.

PIN CONFIGURATION

RGE PACKAGE[(1)]
QFN-24
(TOP VIEW)



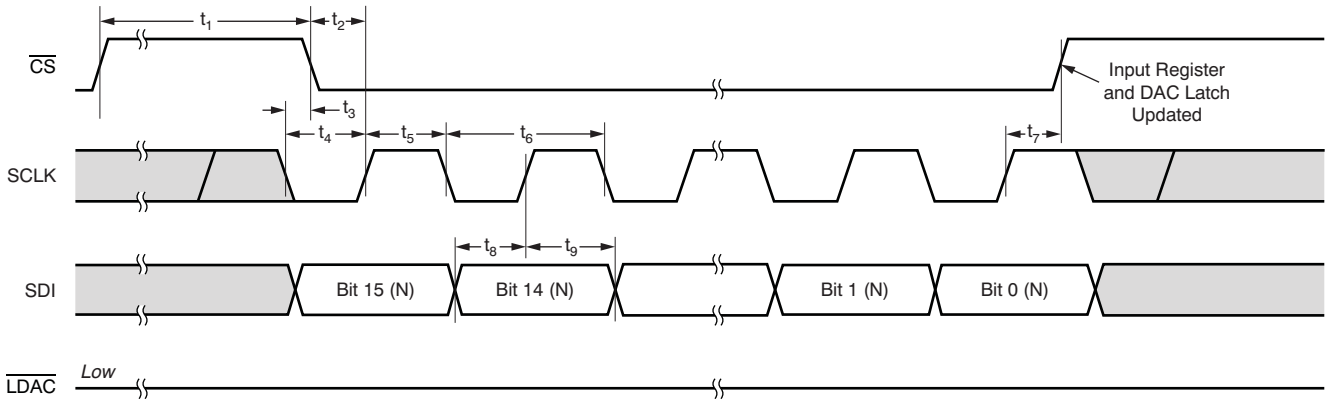
(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1	SCLK	I	SPI bus serial clock input
2	SDI	I	SPI bus serial data input
3	$\overline{\text{LDAC}}$	I	Load DAC latch control input (active low). When $\overline{\text{LDAC}}$ is low, the DAC latch is transparent, and the contents of the input register are transferred to the DAC latch. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated.
4	AGND	I	Analog ground
5	AV_{DD}	I	Analog power supply
6	V_{REFL}-S	I	Reference low input sense
7	V_{REFH}-S	I	Reference high input sense
8	V_{OUT}	O	Output of output buffer
9	R_{FB}	I	Feedback resistor connected to the inverting input of the output buffer.
10	V_{REFL}-F	I	Reference low input force
11	V_{REFH}-F	I	Reference high input force
12	NC	—	Do not connect.
13	NC	—	Do not connect.
14	RSTSEL	I	Selects the value of the output from the V_{OUT} pin after power-on or hardware reset. If RSTSEL = IOV_{DD}, then register data = 8000h. If RSTSEL = DGND, then register data = 0000h.
15	GAIN	I	Buffer gain setting. Gain = 1 when the pin is connected to DGND; Gain = 2 when the pin is connected to IOV_{DD}.
16	USB/$\overline{\text{BTC}}$	I	Input data format selection. Input data are straight binary format when the pin is connected to IOV_{DD}, and in two's complement format when the pin is connected to DGND.
17	$\overline{\text{RST}}$	I	Reset input (active low). Logic low on this pin causes the device to perform a reset.
18	PDN	I	Power-down input (active high). Logic high on this pin forces the device into power-down status. In power-down, the V_{OUT} pin connects to AGND through 10kΩ resistor.
19	$\overline{\text{CS}}$	I	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, SDO is in high-impedance status.
20	SDOSEL	I	SPI serial data output selection. When SDOSEL is tied to IOV_{DD}, the contents of the existing input register are shifted out from the SDO pin; this is Stand-Alone mode. When SDOSEL is tied to DGND, the contents in the SPI input shift register are shifted out from the SDO pin; this is Daisy-Chain mode for daisy chaining communication.
21	DV_{DD}	I	Digital power supply (connect to AV_{DD}, pin 5)
22	DGND	I	Digital ground
23	SDO	O	SPI bus serial data output. Refer to the *Timing Diagrams* for further detail.
24	IOV_{DD}	I	Interface power. Connect to +1.8V for 1.8V logic, +3V for 3V logic, and to +5V for 5V logic.

TIMING DIAGRAMS

Case 1: Standalone operation without SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation without SDO, $\overline{\text{LDAC}}$ active.

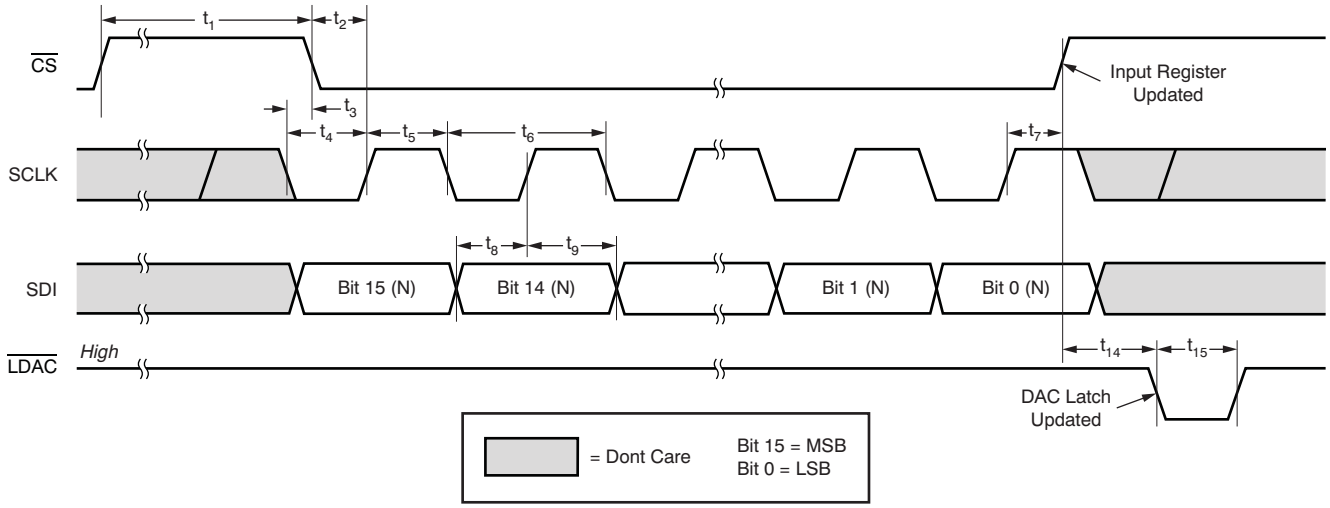


Figure 1. Timing Diagram of Standalone Operation without SDO

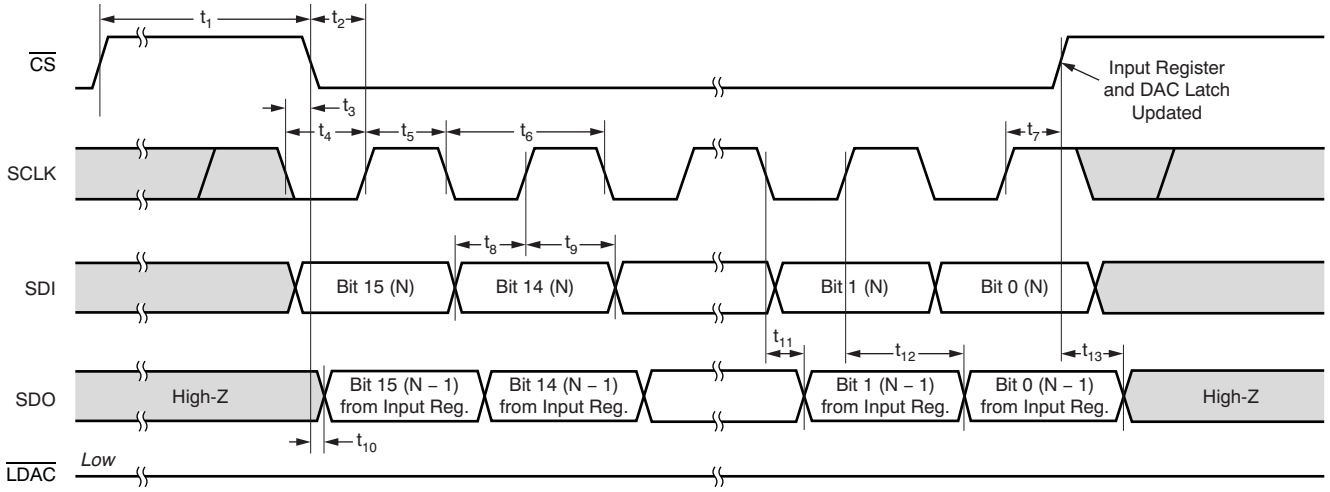
TIMING CHARACTERISTICS for Figure 1 (1)(2)(3)

At –40°C to +105°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		40	MHz
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		50	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	30		ns
t_2	$\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
t_3	SCLK falling edge to $\overline{CS}$ falling edge setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_4	SCLK low time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_5	SCLK high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_6	SCLK cycle time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_7	SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{14}	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse width	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F$ = 2ns (10% to 90% of IOV_{DD}) and timed from a voltage level of $IOV_{DD}/2$.
(2) Ensured by design. Not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

Case 1: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ tied low.



Case 2: Standalone operation with output from SDO, $\overline{\text{LDAC}}$ active.

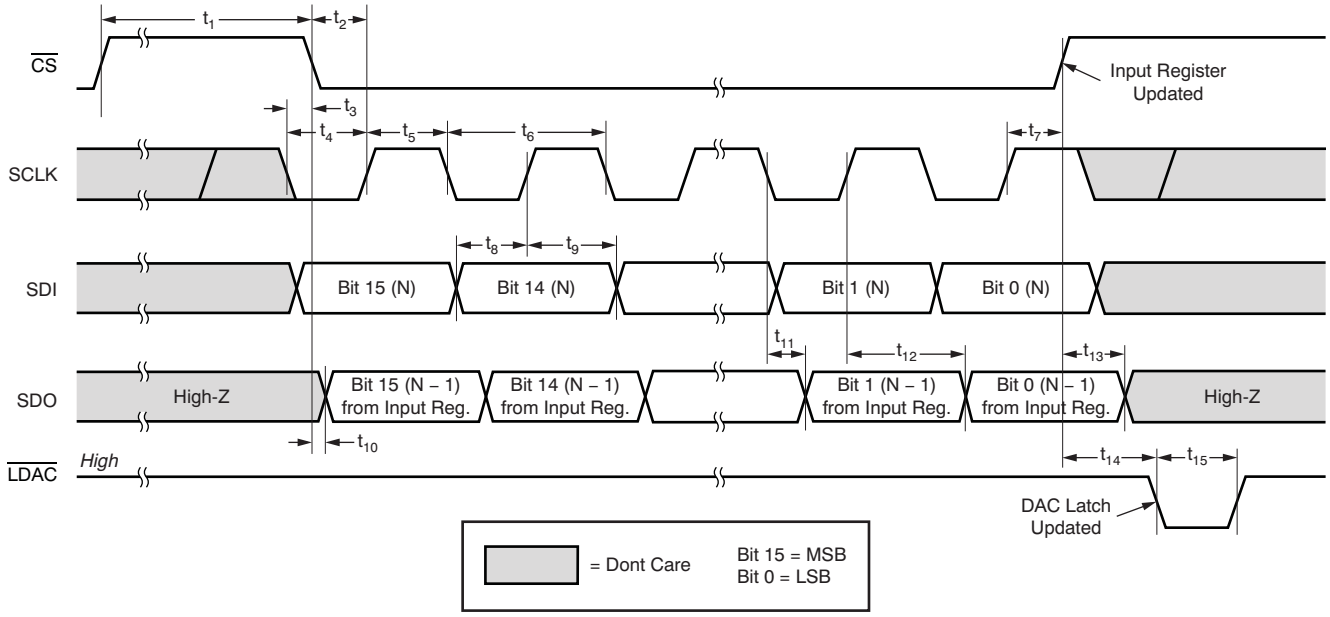
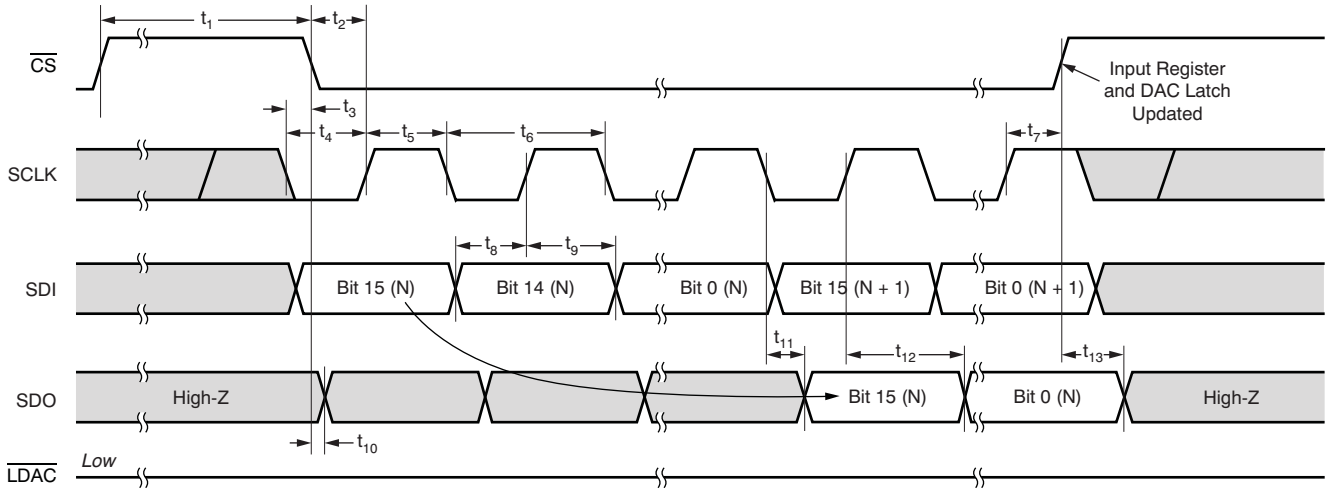


Figure 2. Timing Diagram of Standalone Operation with SDO

Case 1: Daisy Chain, $\overline{\text{LDAC}}$ tied low.



Case 2: Daisy Chain, $\overline{\text{LDAC}}$ active.

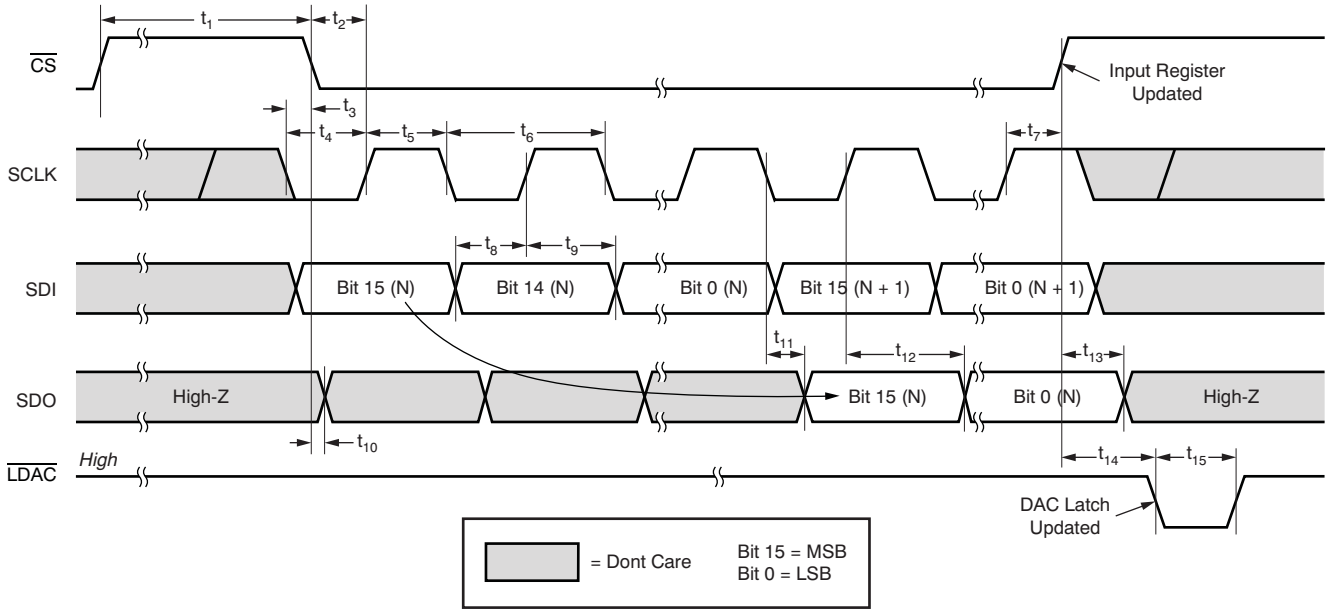


Figure 3. Timing Diagram of Daisy Chain Mode, Two Cascaded Devices

TIMING CHARACTERISTICS for Figure 2 and Figure 3[1][2][3]

At –40°C to +105°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Maximum clock frequency	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		20	MHz
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		25	MHz
t_1	Minumum $\overline{CS}$ high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	30		ns
t_2	$\overline{CS}$ falling edge to SCLK rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	8		ns
t_3	SCLK falling edge to $\overline{CS}$ falling edge setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_4	SCLK low time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_5	SCLK high time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_6	SCLK cycle time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	50		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	40		ns
t_7	SCLK rising edge to $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
t_8	Input data setup time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_9	Input data hold time	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{10}	SDO active from $\overline{CS}$ falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		15	ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		10	ns
t_{11}	SDO data valid from SCLK falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		20	ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		15	ns
t_{12}	SDO data hold from SCLK rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	25		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	20		ns
t_{13}	SDO High-Z from $\overline{CS}$ rising edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$		8	ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$		5	ns
t_{14}	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	5		ns
t_{15}	$\overline{LDAC}$ pulse width	$2.7 \le DV_{DD} < 3.6V$, $2.7 \le IOV_{DD} \le DV_{DD}$	15		ns
		$3.6 \le DV_{DD} \le 5.5V$, $2.7 \le IOV_{DD} \le DV_{DD}$	10		ns

(1) All input signals are specified with $t_R = t_F = 2ns$ (10% to 90% of IOV_{DD}) and timed from a voltage level of $IOV_{DD}/2$.
(2) Ensured by design. Not production tested.
(3) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.

TYPICAL CHARACTERISTICS: V_{DD} = +5V

At T_A = +25°C, V_{REFH} = +5.0V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

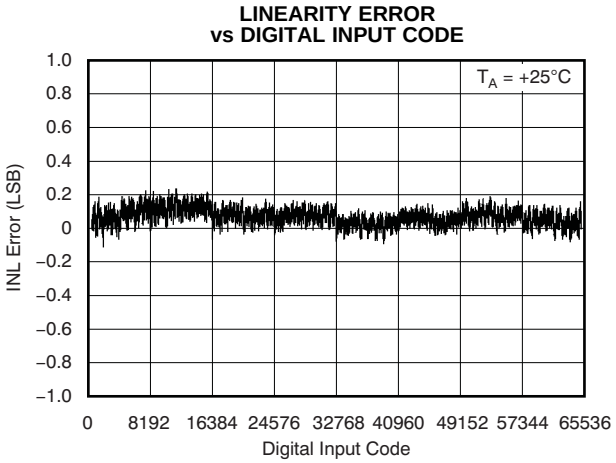


Figure 4.

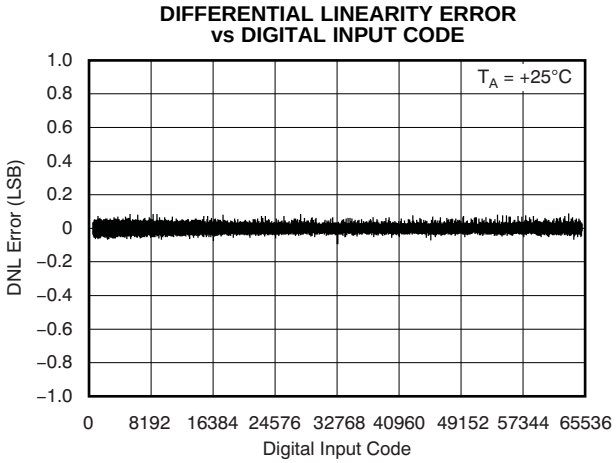


Figure 5.

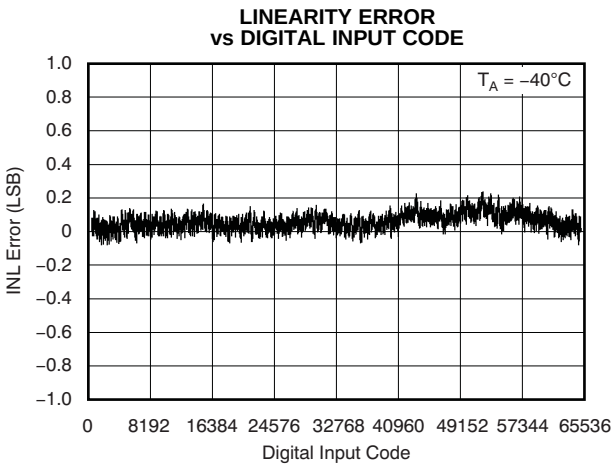


Figure 6.

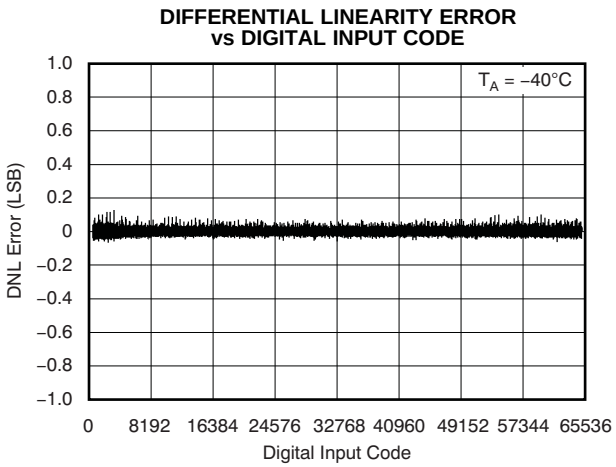


Figure 7.

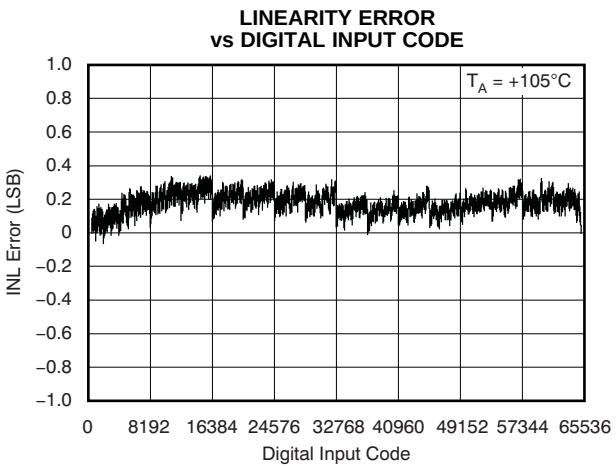


Figure 8.

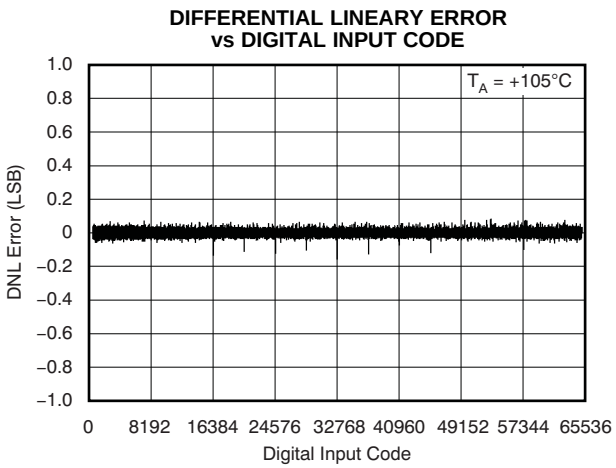


Figure 9.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{REFH} = +5.0V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

LINEARITY ERROR vs TEMPERATURE

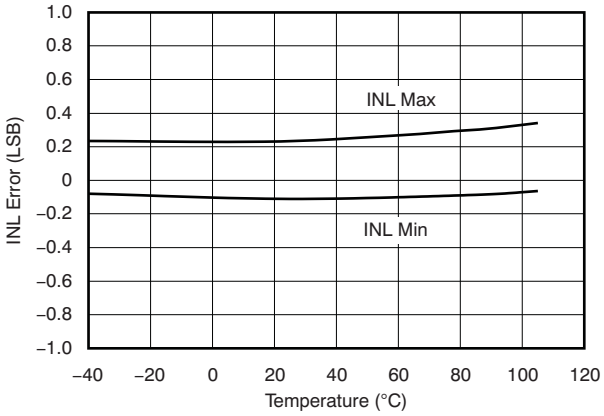


Figure 10.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

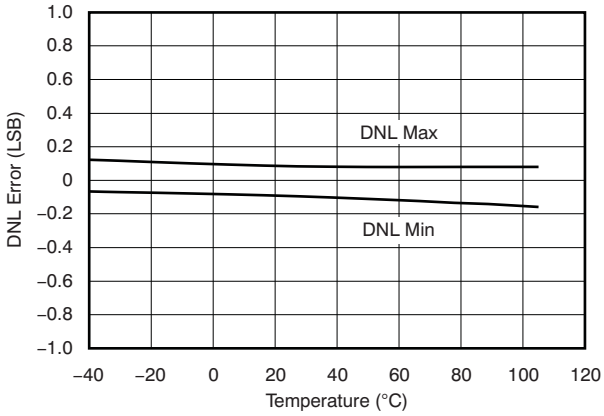


Figure 11.

LINEARITY ERROR vs TEMPERATURE (GAIN = 2X MODE)

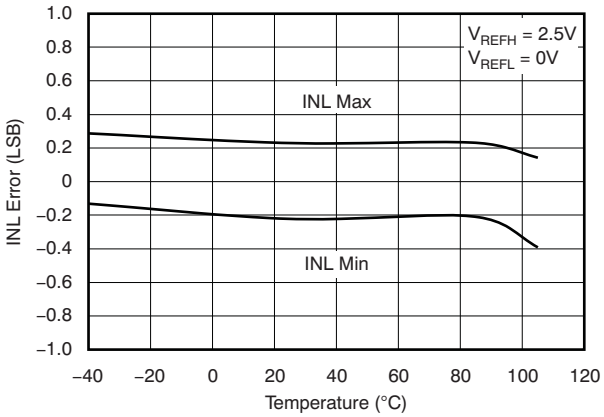


Figure 12.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE (GAIN = 2X MODE)

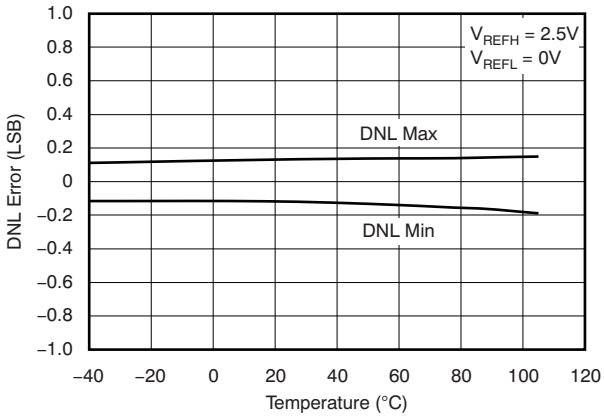


Figure 13.

LINEARITY ERROR vs SUPPLY VOLTAGE

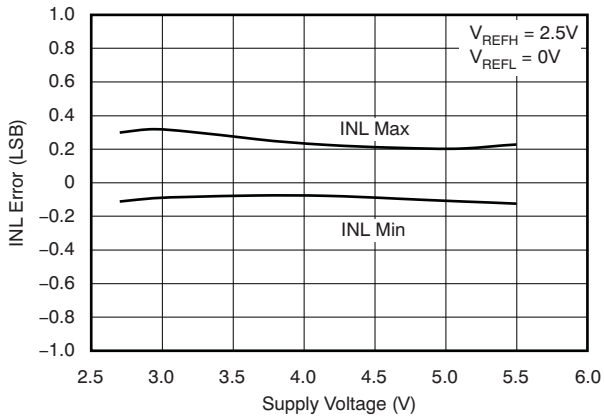


Figure 14.

DIFFERENTIAL LINEARITY ERROR vs SUPPLY VOLTAGE

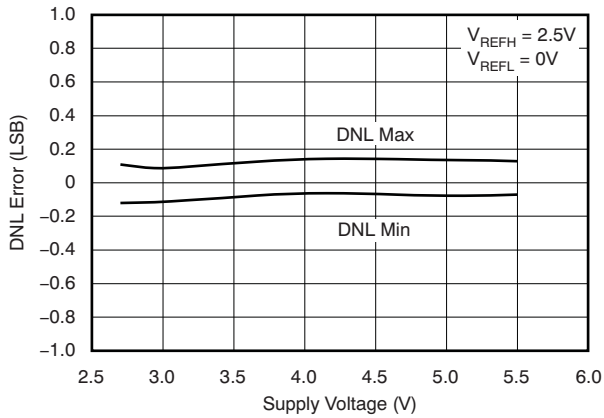


Figure 15.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{REFH} = +5.0V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

LINEARITY ERROR vs REFERENCE VOLTAGE

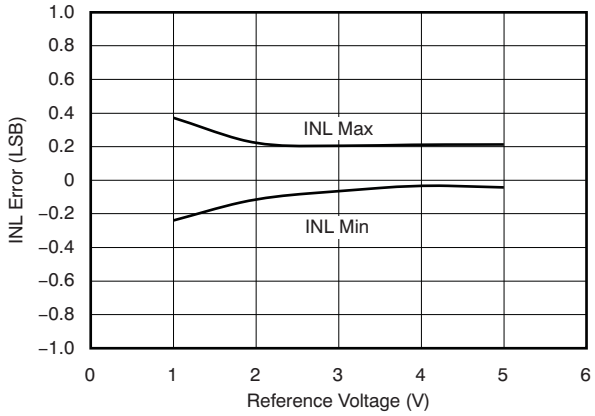


Figure 16.

DIFFERENTIAL LINEARITY ERROR vs REFERENCE VOLTAGE

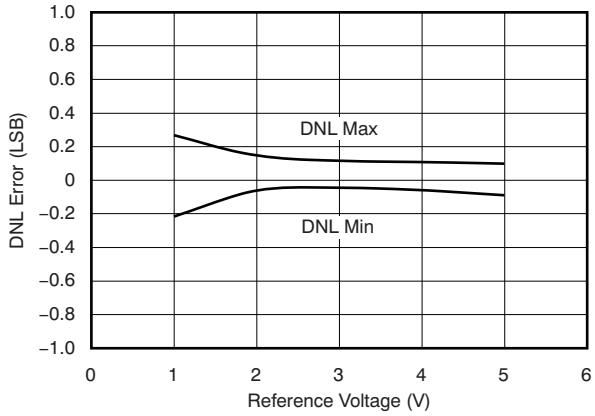


Figure 17.

ENDPOINT ERROR vs TEMPERATURE

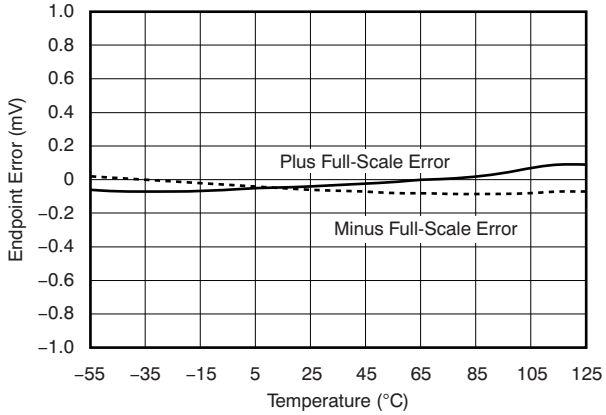


Figure 18.

ENDPOINT ERROR vs TEMPERATURE (GAIN = 2X MODE)

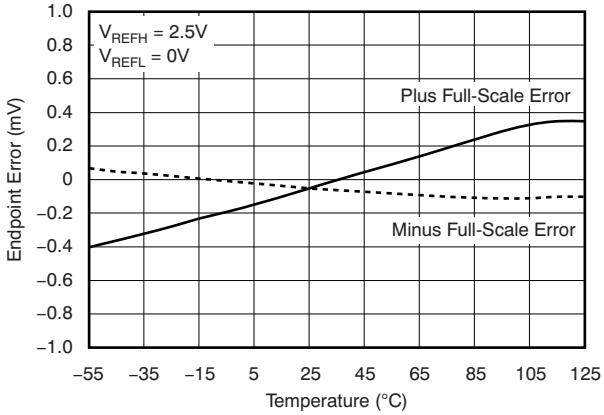


Figure 19.

AV_{DD} SUPPLY CURRENT vs DIGITAL INPUT CODE

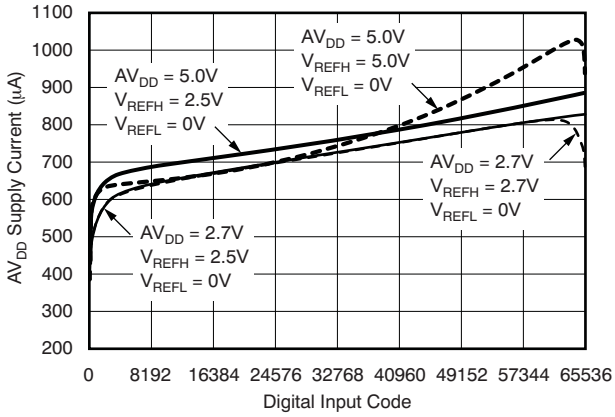


Figure 20.

AV_{DD} SUPPLY CURRENT vs DIGITAL INPUT CODE (GAIN = 2X MODE)

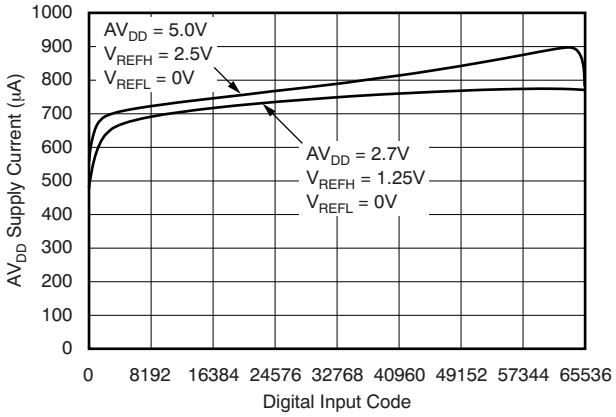


Figure 21.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{REFH} = +5.0V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

AV_{DD} SUPPLY CURRENT vs TEMPERATURE

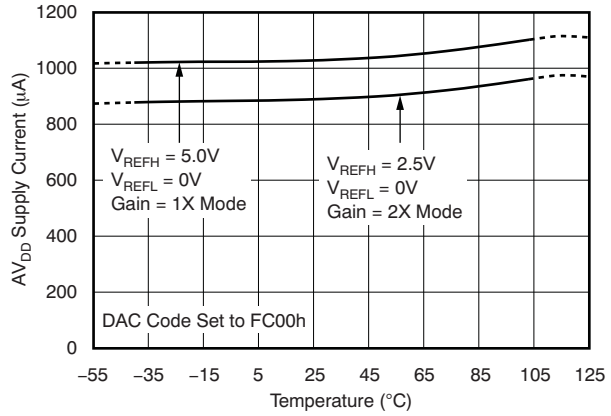


Figure 22.

AV_{DD} POWER-DOWN CURRENT vs TEMPERATURE

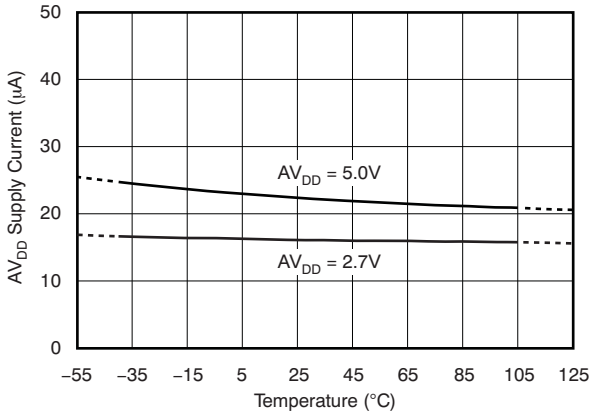


Figure 23.

REFERENCE CURRENT vs DIGITAL INPUT CODE

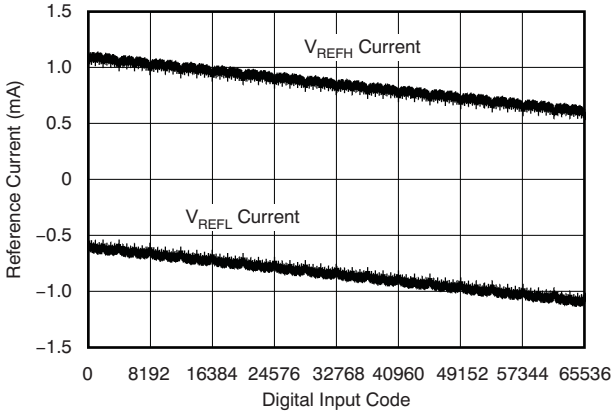


Figure 24.

REFERENCE CURRENT vs DIGITAL INPUT CODE (GAIN = 2X MODE)

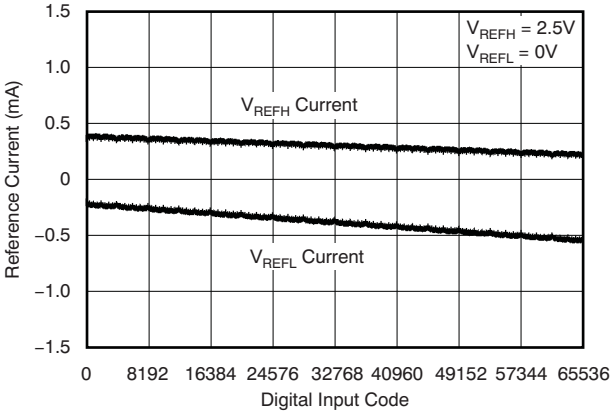


Figure 25.

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY

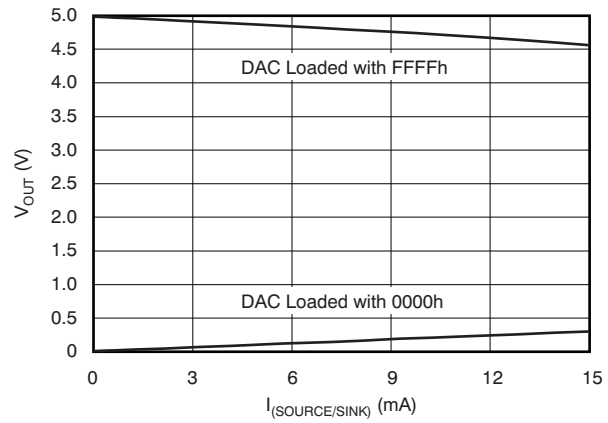


Figure 26.

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY (Operation Near AV_{DD} Rail)

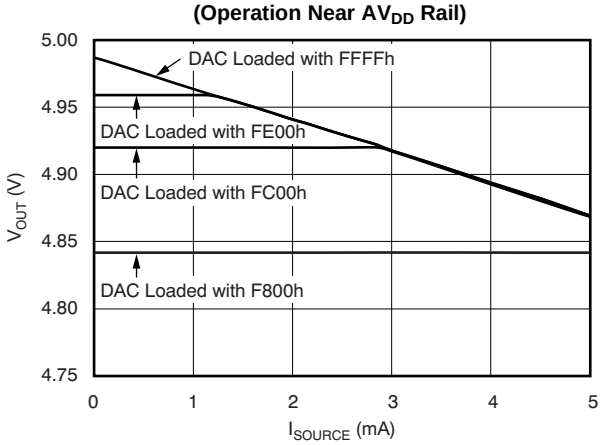


Figure 27.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{REFH} = +5.0V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY (Operation Near AGND Rail)

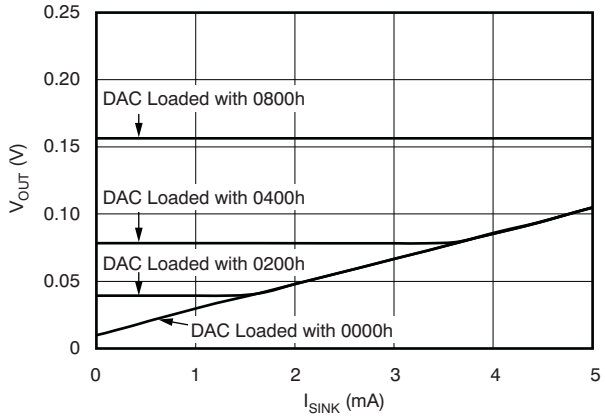


Figure 28.

IOV_{DD} SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

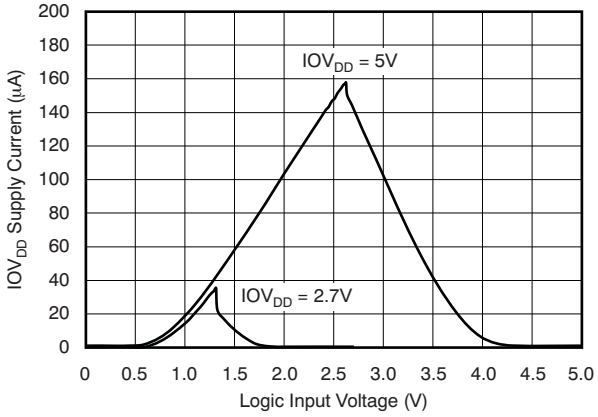


Figure 29.

LARGE SIGNAL SETTLING TIME

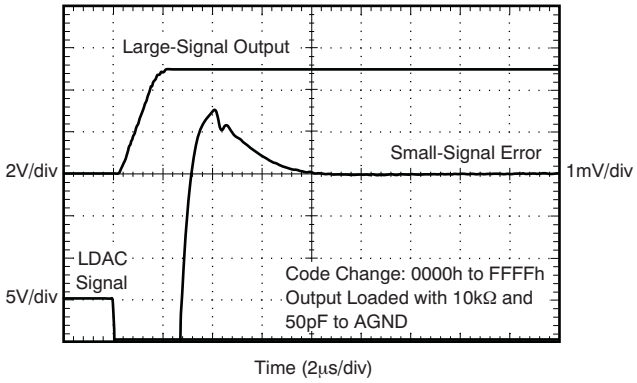


Figure 30.

LARGE SIGNAL SETTLING TIME

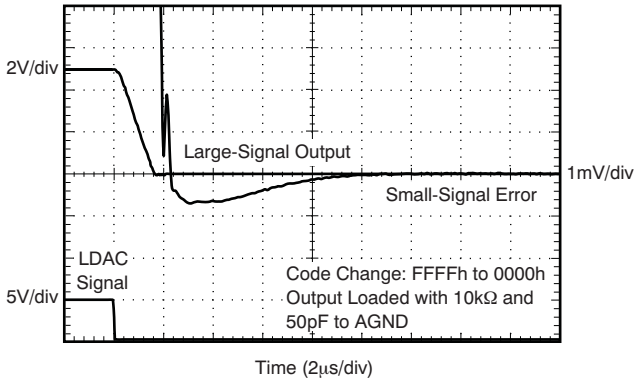


Figure 31.

LARGE SIGNAL SETTLING TIME

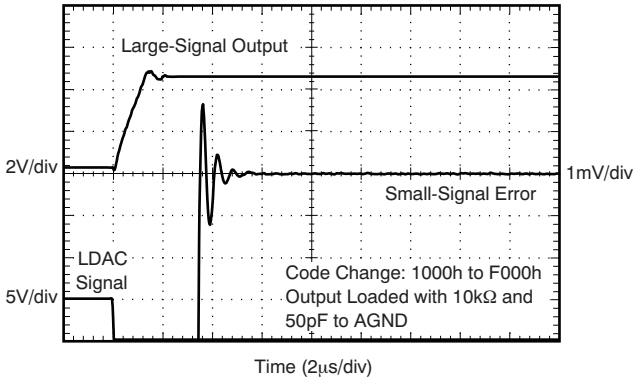


Figure 32.

LARGE SIGNAL SETTLING TIME

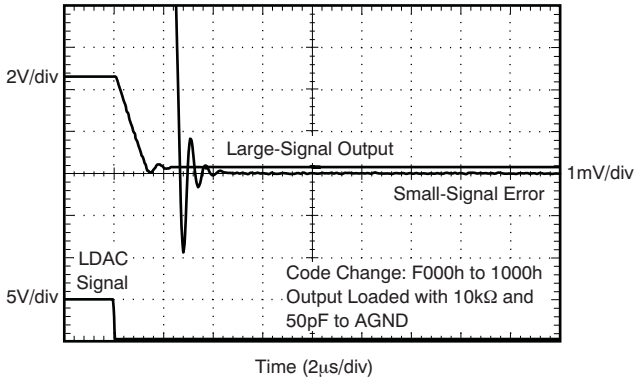


Figure 33.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{REFH} = +5.0V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

LARGE SIGNAL SETTLING TIME (GAIN = 2X MODE)

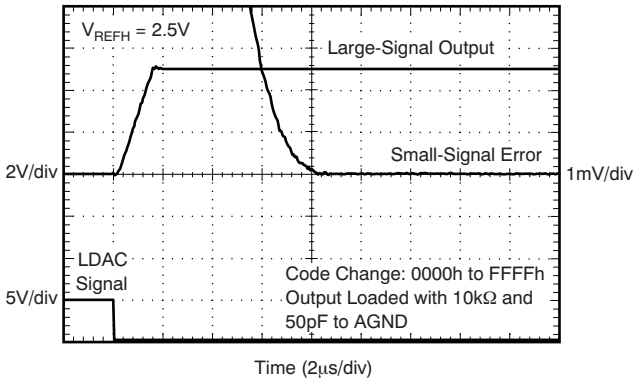


Figure 34.

LARGE SIGNAL SETTLING TIME (GAIN = 2X MODE)

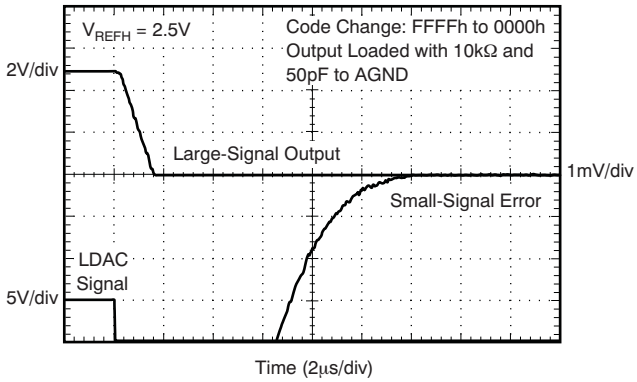


Figure 35.

LARGE SIGNAL SETTLING TIME (GAIN = 2X MODE)

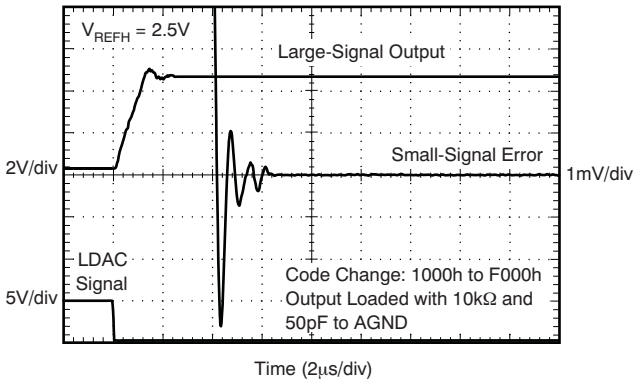


Figure 36.

LARGE SIGNAL SETTLING TIME (GAIN = 2X MODE)

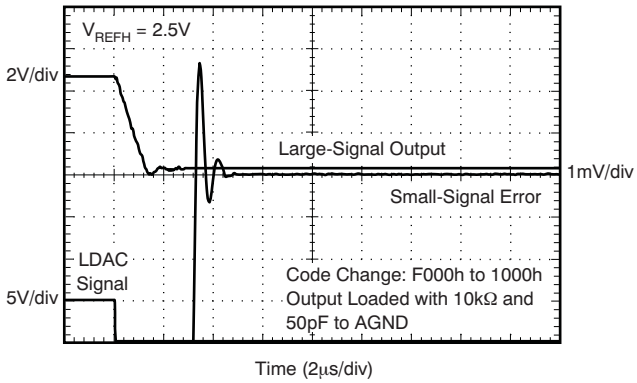


Figure 37.

MAJOR CARRY GLITCH

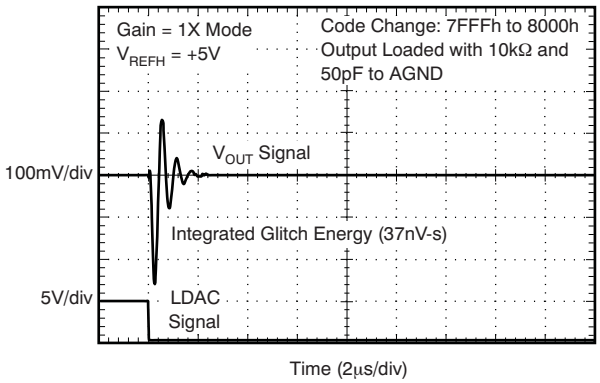


Figure 38.

MAJOR CARRY GLITCH

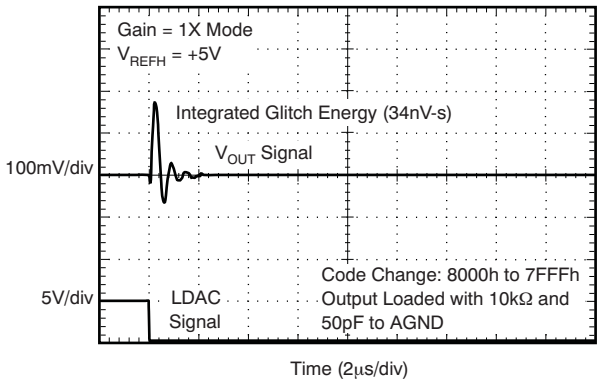


Figure 39.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{REFH} = +5.0V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

MAJOR CARRY GLITCH

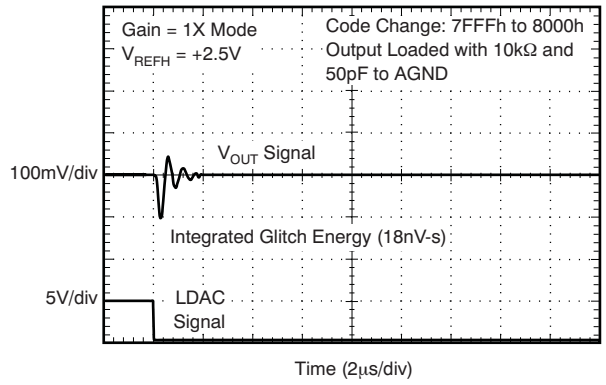


Figure 40.

MAJOR CARRY GLITCH

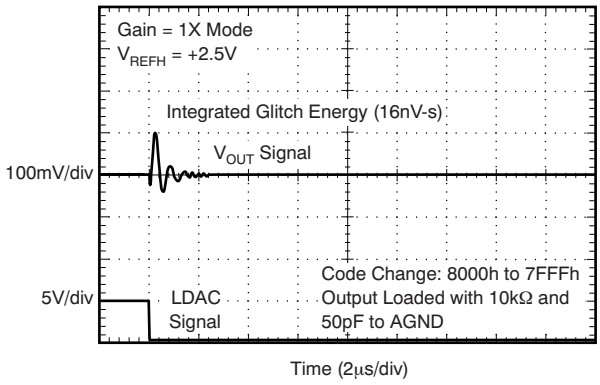


Figure 41.

OUTPUT NOISE DENSITY vs FREQUENCY

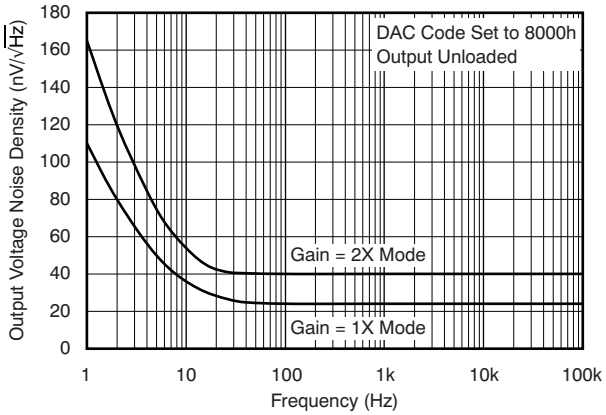


Figure 42.

LOW-FREQUENCY OUTPUT NOISE (0.1Hz to 10Hz)

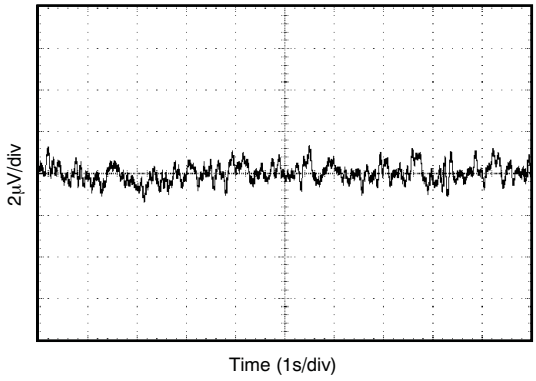


Figure 43.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At T_A = +25°C, V_{REFH} = +2.5V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

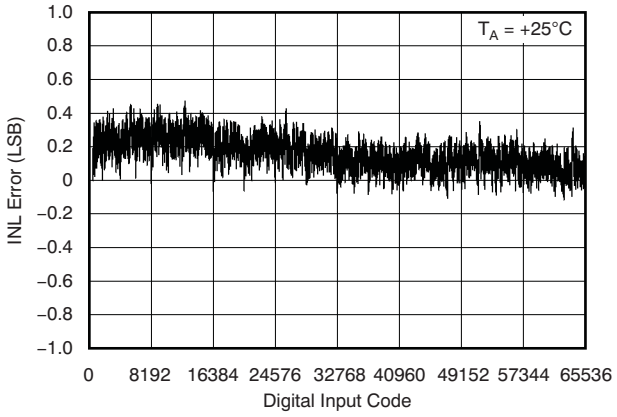


Figure 44.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

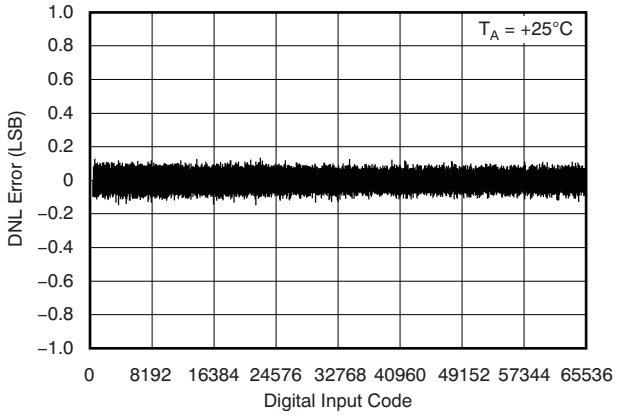


Figure 45.

LINEARITY ERROR vs DIGITAL INPUT CODE

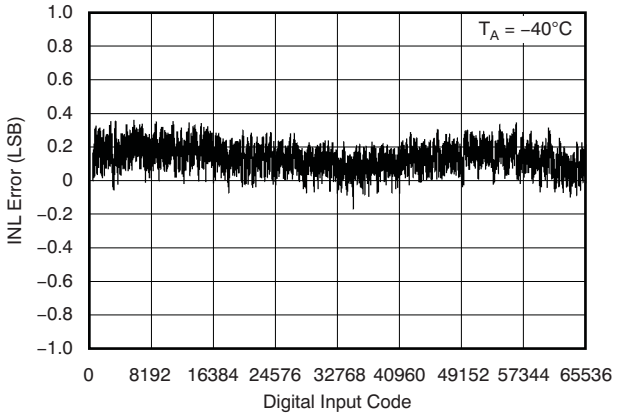


Figure 46.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

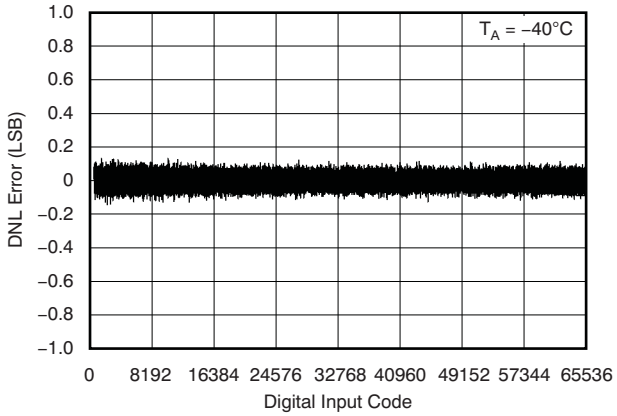


Figure 47.

LINEARITY ERROR vs DIGITAL INPUT CODE

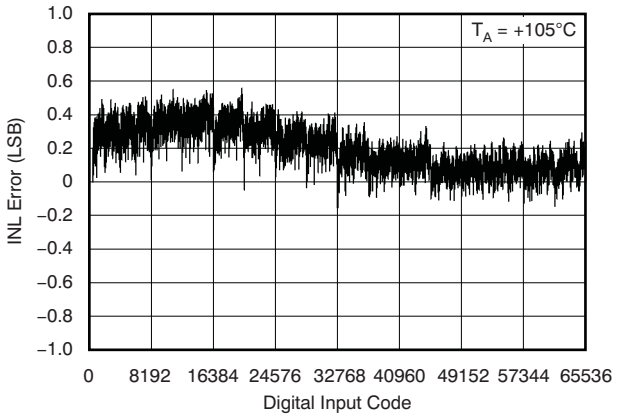


Figure 48.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

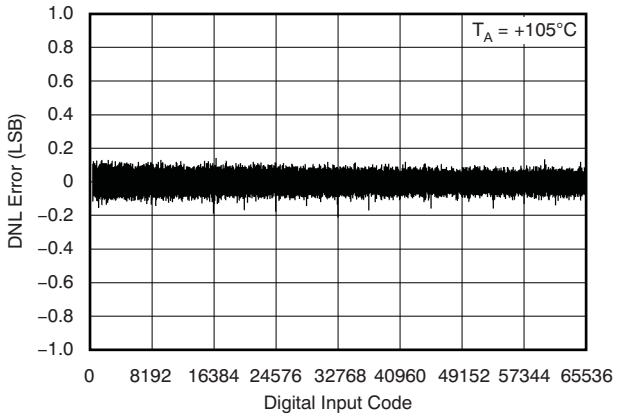


Figure 49.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, V_{REFH} = +2.5V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

LINEARITY ERROR vs REFERENCE VOLTAGE

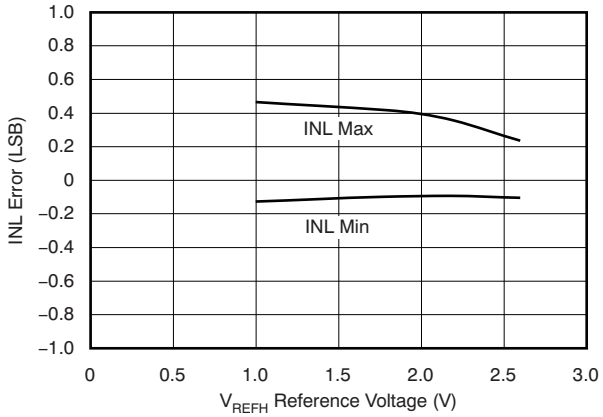


Figure 50.

DIFFERENTIAL LINEARITY ERROR vs REFERENCE VOLTAGE

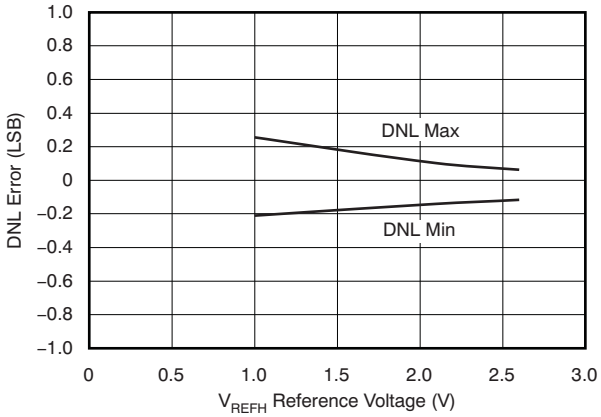


Figure 51.

AV_{DD} SUPPLY CURRENT vs TEMPERATURE

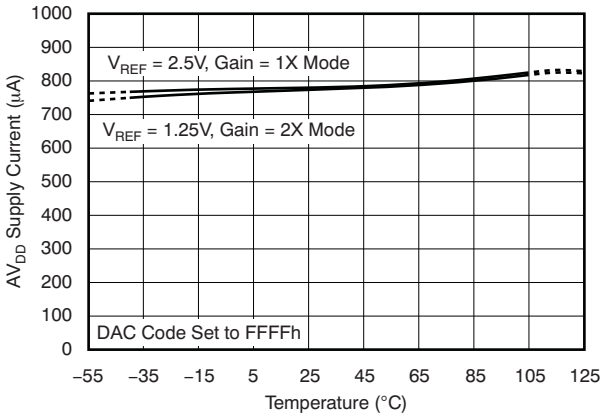


Figure 52.

REFERENCE CURRENT vs DIGITAL INPUT CODE

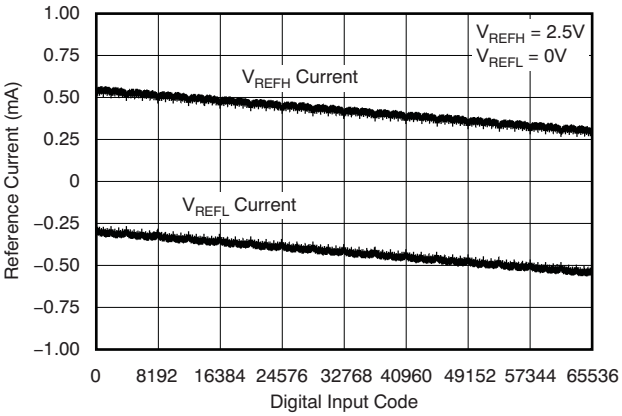


Figure 53.

REFERENCE CURRENT vs DIGITAL INPUT CODE (GAIN = 2X MODE)

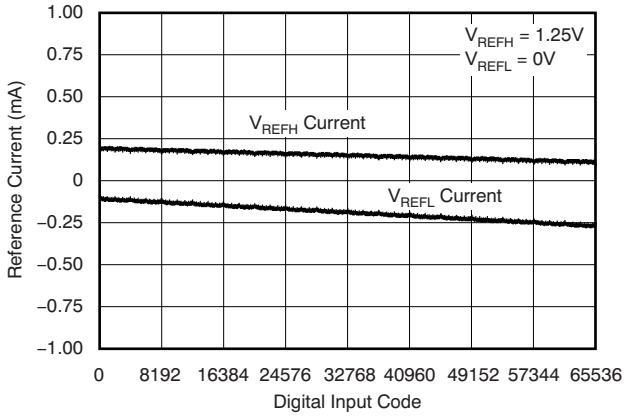


Figure 54.

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY

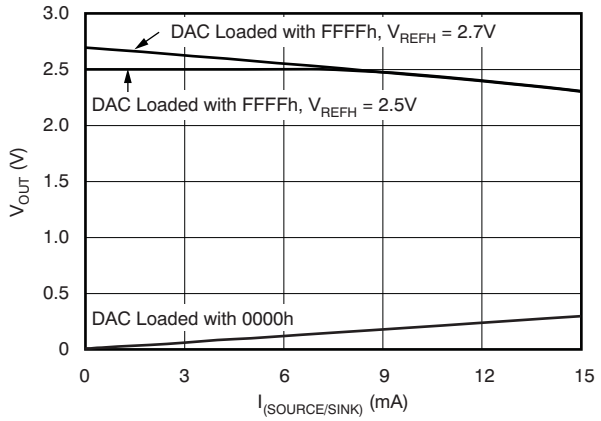


Figure 55.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, V_{REFH} = +2.5V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY (Operation Near AV_{DD} Rail)

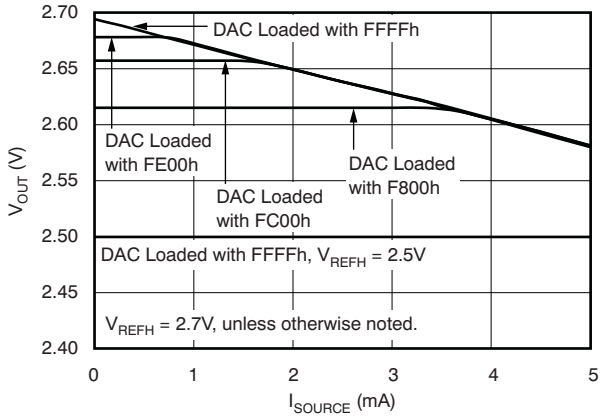


Figure 56.

OUTPUT VOLTAGE vs DRIVE CURRENT CAPABILITY (Operation Near AGND Rail)

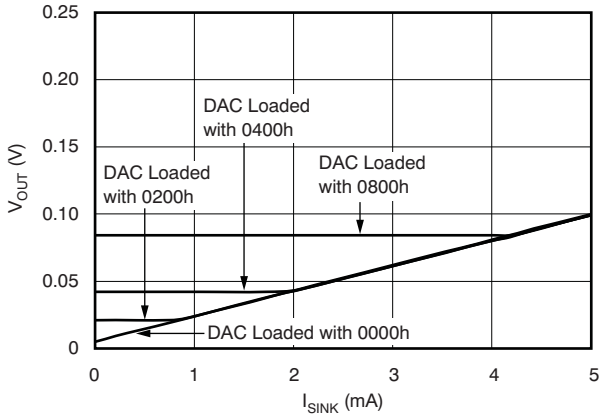


Figure 57.

LARGE SIGNAL SETTLING TIME

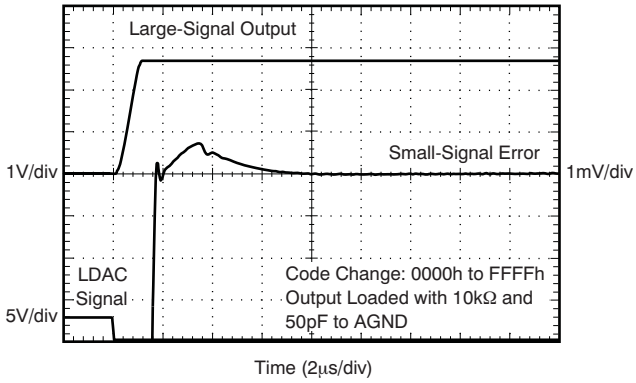


Figure 58.

LARGE SIGNAL SETTLING TIME

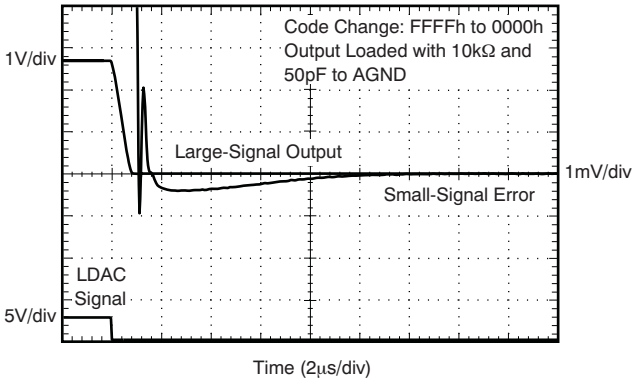


Figure 59.

LARGE SIGNAL SETTLING TIME

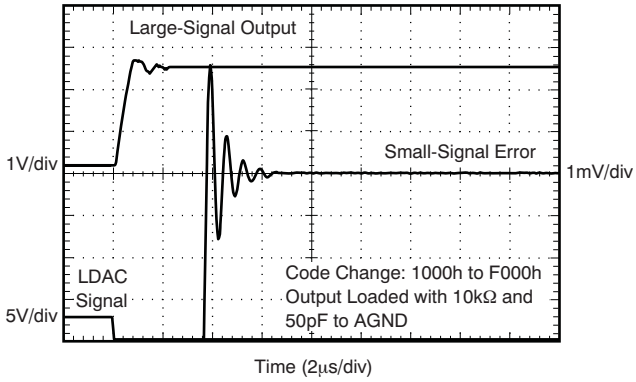


Figure 60.

LARGE SIGNAL SETTLING TIME

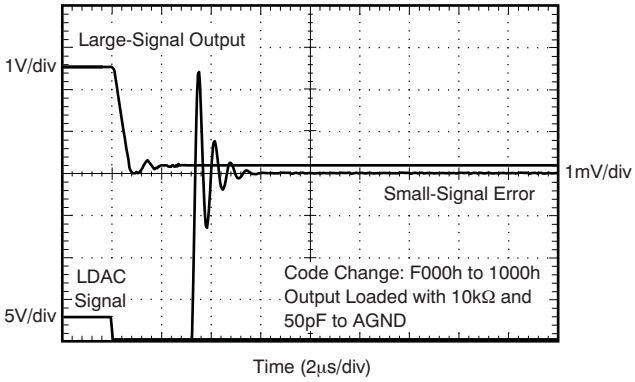


Figure 61.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, V_{REFH} = +2.5V, V_{REFL} = 0V, and Gain = 1X Mode, unless otherwise noted.

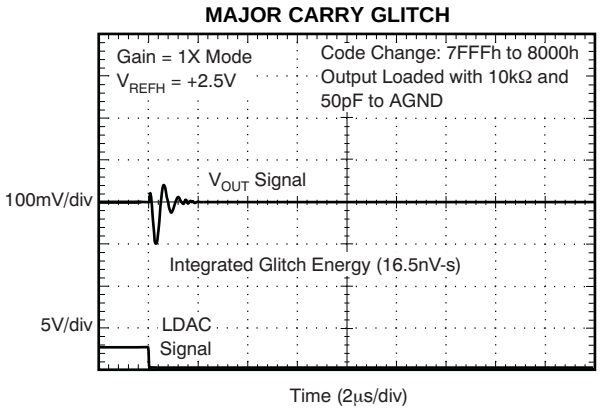


Figure 62.

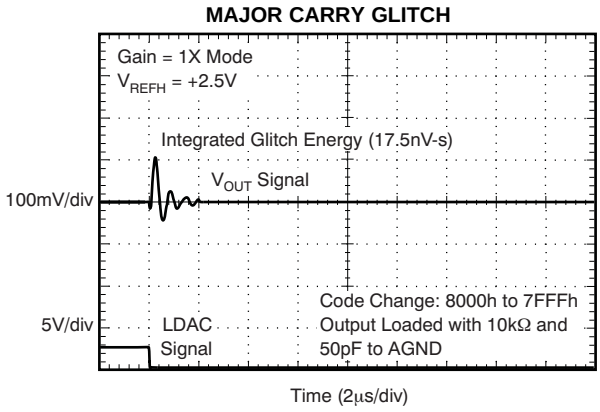


Figure 63.

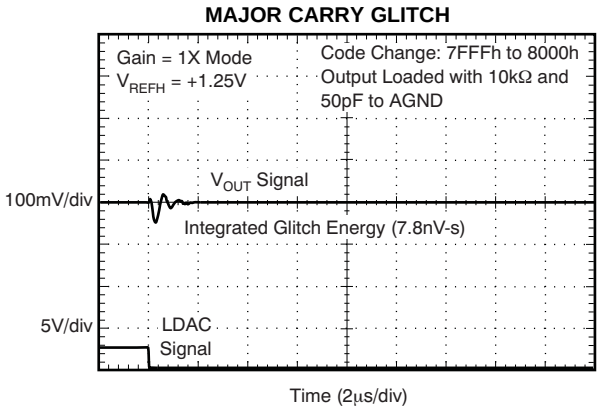


Figure 64.

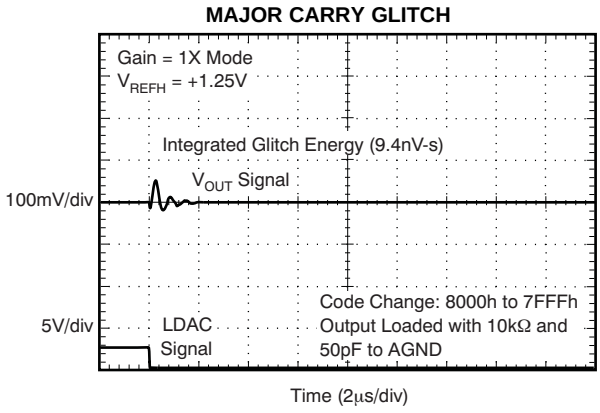


Figure 65.

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8881 is a single-channel, 16-bit, serial-input, voltage-output digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the four MSBs segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 66. The on-chip output buffer allows rail-to-rail output swings while providing a low output impedance to drive loads. The DAC8881 operates from a single analog power supply that ranges from 2.7V to 5.5V, and typically consumes 850µA when operating with a 3V supply. Data are written to the device in a 16-bit word format, via an SPI serial interface. To enable compatibility with 1.8V, 3V, or 5V logic families, an IOV_{DD} supply pin is provided. This pin allows the DAC8881 input and output logic to be powered from the same logic supply used to interface signals to and from the device. Internal voltage translators are included in the DAC8881 to interface digital signals to the device core. Separate AV_{DD} and DV_{DD} supply pins are provided, but should be connected together. See Figure 67 for the basic configuration of the DAC8881.

To ensure a known power-up state, the DAC8881 is designed with a power-on reset function. Upon power-up, the DAC8881 is reset to either zero-scale or midscale depending on the state of the RSTSEL pin. The device can also be hardware reset by using the $\overline{RST}$ and RSTSEL pins.

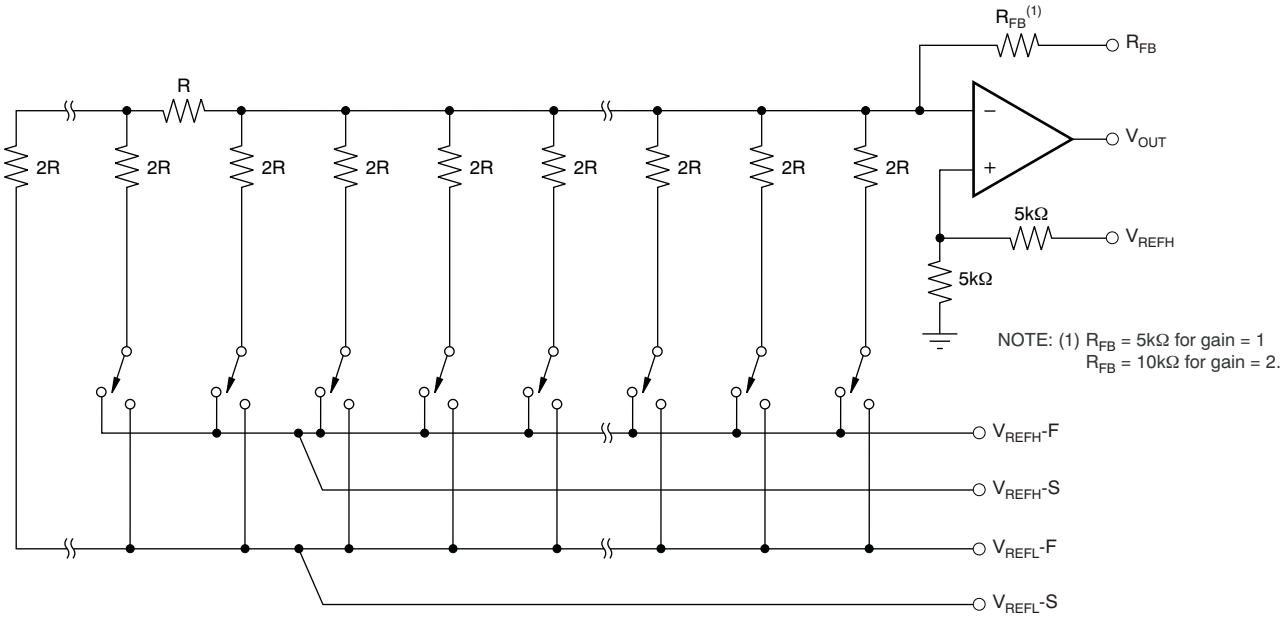


Figure 66. DAC8881 Architecture

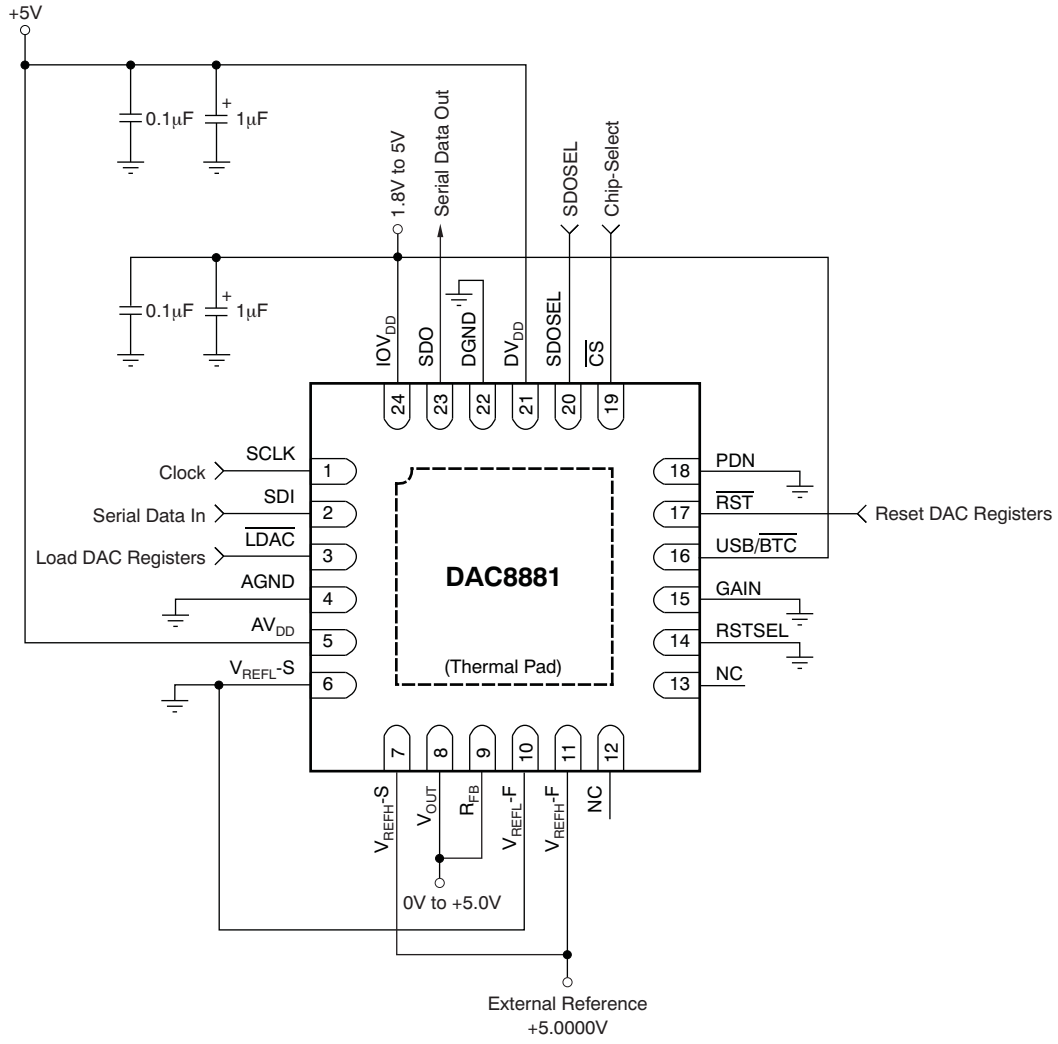


Figure 67. Basic Configuration

ANALOG OUTPUT

The DAC8881 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 68), thus ensuring an accurate output voltage. The output buffer V_{OUT} and R_{FB} pins are provided so that the output op amp buffer feedback can be connected at the load. Without a driven load, the DAC8881 output typically swings to within 15mV of the AGND and AV_{DD} supply rails. Because of the high accuracy of these DACs, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 5V full-scale range has a 1LSB value of 76µV. With a load current of 1mA, a series wiring and connector resistance of only 80mΩ (R_{W2}) causes a voltage drop of 80µV. In terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is 0.5mΩ per square. For a 1mA load, a 0.25mm wide printed circuit conductor 25mm long results in a voltage drop of 50µV.

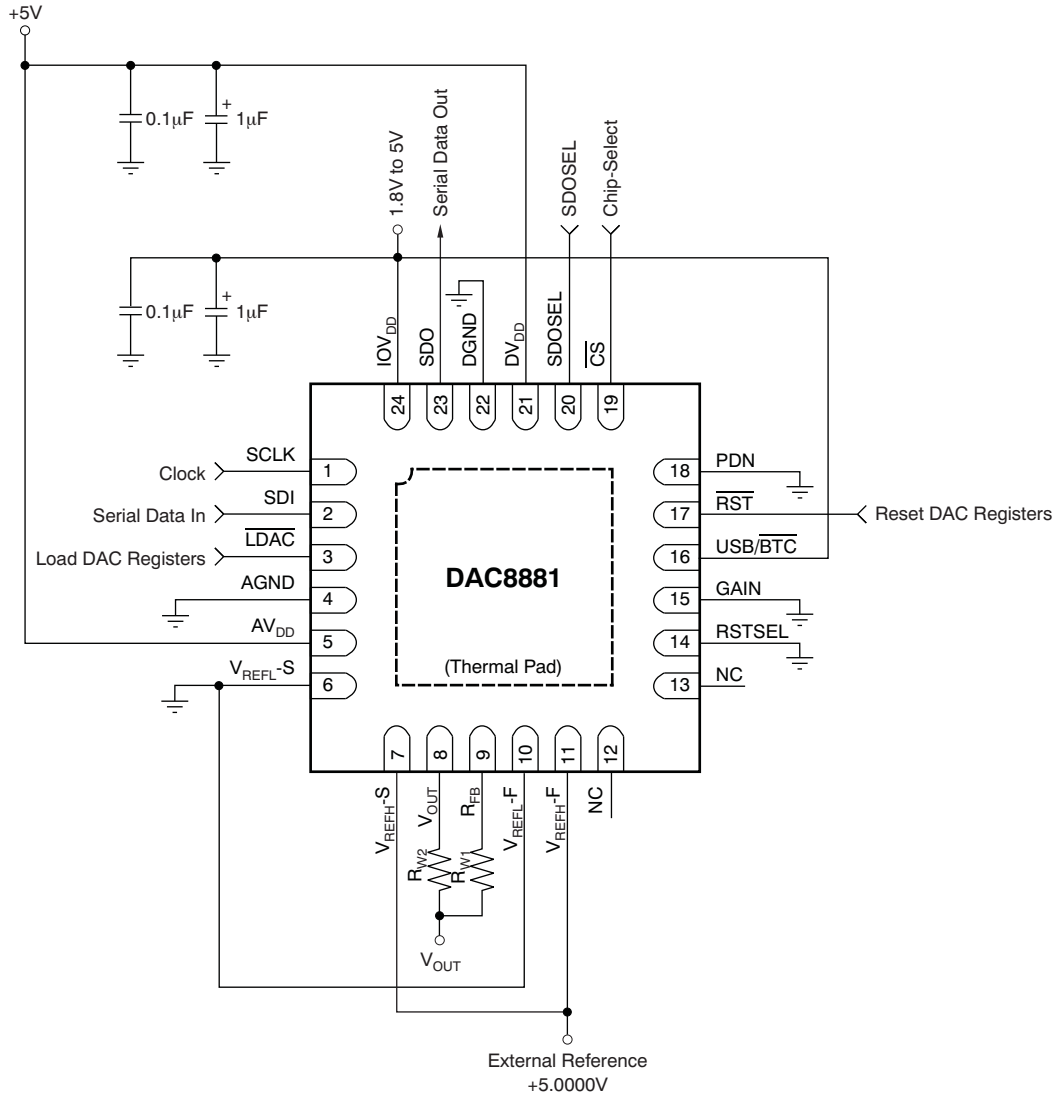


Figure 68. Analog Output Closed-Loop Configuration (R_{W1} and R_{W2} represent wiring resistance)

REFERENCE INPUTS

The reference high input, V_{REFH}, can be set to any voltage in the range of 1.25V to AV_{DD}. The reference low input, V_{REFL}, can be set to any voltage in the range of –0.2V to +0.2V (to provide a small offset to the output of the DAC8881, if desired). The current into V_{REFH} and out of V_{REFL} depends on the DAC code, and can vary from approximately 0.5mA to 1mA in the gain = 1X mode of operation. The reference high and low inputs appear as varying loads to the external reference circuit. If the external references can source or sink the required current, and if low impedance connections are made to the V_{REFH} and V_{REFL} pins, external reference buffers are not required. Figure 67 shows a simple configuration of the DAC8881 using external references without force/sense reference buffers.

Kelvin sense connections for the reference high and low are included on the DAC8881. When properly used with external reference buffer op amps, these reference Kelvin sense pins ensure that the driven reference high and low voltages remain stable versus varying reference load currents. Figure 69 shows an example of a reference force/sense configuration of the DAC8881 operating from a single analog supply voltage. Both the V_{REFL} and V_{REFH} reference voltages are set to levels of 100mV from the DAC8881 supply rails, and are derived from a +5V external reference. Figure 71 and Figure 70 illustrate the effect of not using the reference force/sense buffers to drive the DAC8881 V_{REFL} and V_{REFH} pins. A slight degradation in INL and DNL performance of approximately 0.1 LSB may be seen without the use of the force/sense buffer configuration.

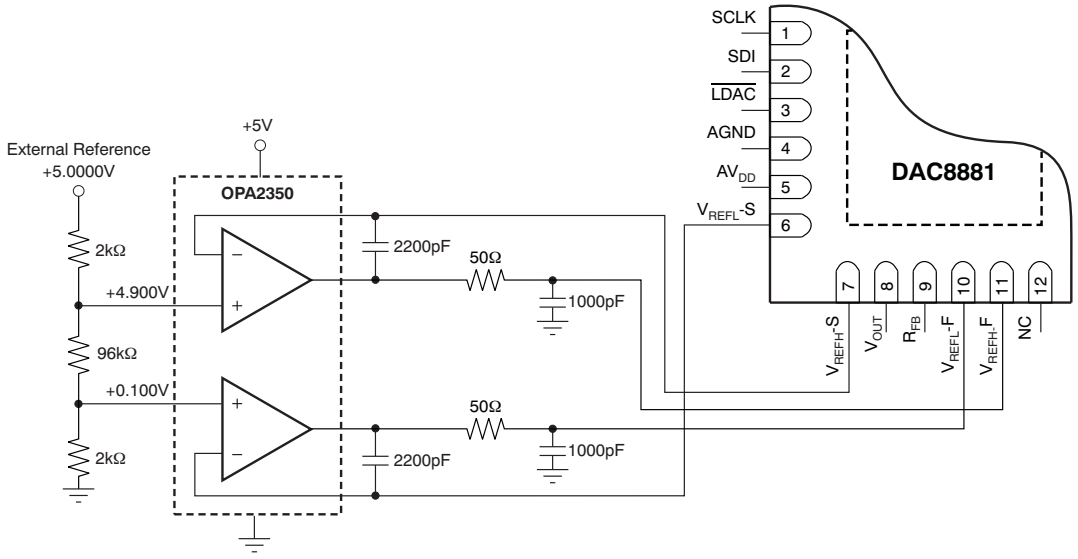


Figure 69. Buffered References (V_{REFH} = +4.900V and V_{REFL} = 100mV)

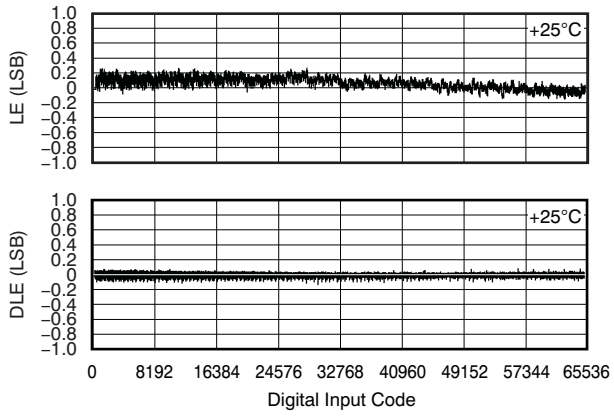


Figure 70. Linearity and Differential Linearity Error for Figure 67 without Reference Buffers

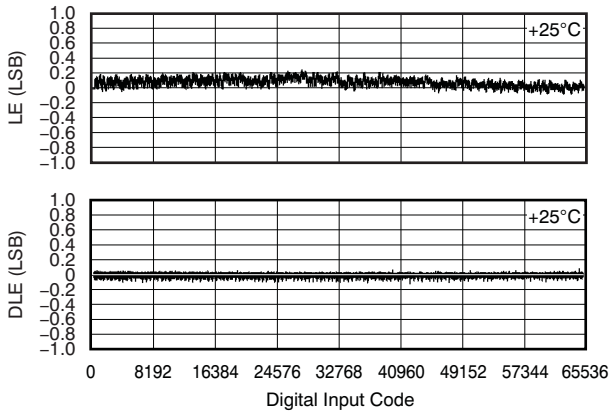


Figure 71. Linearity and DifferentialLinearity Error for Figure 69 with Reference Buffers

OUTPUT RANGE

The maximum output range of the DAC8881 is V_{REFL} to $V_{REFH} \times G$, where *G* is the output buffer gain set by the GAIN pin. When the GAIN pin is connected to DGND, the output buffer gain = 1. When the GAIN pin is connected to IOV_{DD}, the output buffer gain = 2. The output range must not be greater than AV_{DD}; otherwise, output saturation occurs. The DAC8881 output transfer function is given in Equation 1:

$$V_{OUT} = \frac{V_{REFH} - V_{REFL}}{65536} \times CODE \times Buffer\ Gain + V_{REFL} \quad (1)$$

Where:

CODE = 0 to 65535. This is the digital code loaded to the DAC.

Buffer Gain = 1 or 2 (set by the GAIN pin).

V_{REFH} = reference high voltage applied to the device.

V_{REFL} = reference low voltage applied to the device.

INPUT DATA FORMAT

The USB/$\overline{BTC}$ pin defines the input data format. When this pin is connected to IOV_{DD}, the input data format is straight binary, as shown in Table 1. When this pin is connected to DGND, the input data format is two's complement, as shown in Table 2.

Table 1. Output vs Straight Binary Code

USB CODE	5V RANGE	DESCRIPTION
FFFFh	+4.99992	+Full-Scale – 1LSB
C000h	+3.75000	3/4-Scale
8000h	+2.50000	Midscale
4000h	+1.25000	1/4-Scale
0000h	0.00000	Zero-Scale

Table 2. Output vs Two's Complement Code

$\overline{BTC}$ CODE	5V RANGE	DESCRIPTION
7FFFh	+4.99992	+Full-Scale – 1LSB
4000h	+3.75000	3/4-Scale
0000h	+2.50000	Midscale
FFFFh	+2.49992	Midscale – 1LSB
C000h	+1.25000	1/4-Scale
8000h	0.00000	Zero-Scale

POWER DOWN

The DAC8881 has a hardware power-down function. When the PDN pin is high, the device is in power-down mode. The V_{OUT} pin is connected to ground through an internal 10kΩ resistor, but the contents of the input register and the DAC latch do not change. In power-down mode, SPI communication is still active.

HARDWARE RESET

When the $\overline{RST}$ pin is low, the device is in hardware reset mode, and the input register and DAC latch are set to the value defined by the RSTSEL pin. After $\overline{RST}$ goes high, the device is in normal operating mode.

POWER-ON RESET

The DAC8881 has a power-on reset function. After power-on, the value of the input register, the DAC latch, and the output from the V_{OUT} pin are set to the value defined by the RSTSEL pin.

PROGRAM RESET VALUE

After a power-on reset or a hardware reset, the output voltage from the V_{OUT} pin and the values of the input register and DAC latch are determined by the status of the RSTSEL pin and the input data format, as shown in Table 3.

Table 3. Reset Value

RSTSEL PIN	USB/$\overline{BTC}$ PIN	INPUT FORMAT	V_{OUT}	VALUE OF INPUT REGISTER AND DAC LATCH
DGND	IOV_{DD}	Straight Binary	0	0000h
IOV_{DD}	IOV_{DD}	Straight Binary	Midscale	8000h
DGND	DGND	Two's Complement	Midscale	0000h
IOV_{DD}	DGND	Two's Complement	0	8000h

SERIAL INTERFACE

The DAC8881 is controlled by a versatile 3-wire serial interface that operates at clock rates of up to 50MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP™ interface standards.

Input Shift Register

Data are loaded into the device as a 16-bit word under the control of the serial clock input, SCLK. The timing diagrams for this operation are shown in the *Timing Diagram* section.

The $\overline{CS}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while $\overline{CS}$ is low. To start the serial data transfer, $\overline{CS}$ should be taken low, observing the minimum $\overline{CS}$ falling edge to SCLK rising edge setup time, t_2. After $\overline{CS}$ goes low, serial data are clocked into the device input shift register on the rising edges of SCLK for 16 or more clock pulses. If a frame contains less than 16 bits of data, the frame is invalid. Invalid data are not written into the input register and DAC, although the input register and DAC will continue to hold data from the preceding valid data cycle. If more than 16 bits of data are transmitted in one frame, the last 16 bits are written into the shift register and DAC. $\overline{CS}$ may be taken high after the rising edge of the 16th SCLK pulse, observing the minimum SCLK rising edge to $\overline{CS}$ rising edge time, t_7. The contents of the shift register are transferred into the input register on the rising edge of $\overline{CS}$. When data have been transferred into the input register of the DAC, the corresponding DAC register and DAC output can be updated by taking the $\overline{LDAC}$ pin low.

Stand-Alone Mode

When the SDOSEL pin is tied to IOV_{DD}, the interface is in Stand-Alone mode. This mode provides serial readback for diagnostic purposes. The new input data (16 bits) are clocked into the device shift register and the existing data in the input register (16 bits) are shifted out from the SDO pin. If more than 16 SCLKs are clocked when $\overline{CS}$ is low, the contents of the input register are shifted out from the SDO pin, followed by zeroes; the last 16 bits of input data remain in the shift register. If less than 16 SCLKs are clocked while $\overline{CS}$ is low, the data from the SDO pin are part of the data in the input register and must be ignored. Refer to Figure 2 for further detail.

Daisy-Chain Mode

When the SDOSEL pin is tied to GND, the interface is in Daisy-Chain mode. For systems that contain several DACs, the SDO pin may be used to daisy-chain several devices together.

In Daisy-Chain mode, SCLK is continuously applied to the input shift register while $\overline{CS}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. These data are clocked out on the falling edge of SCLK and are valid on the rising edge. By connecting this line to the DIN input

on the next DAC in the chain, a multi-DAC interface is constructed. 16 clock pulses are required for each DAC in the system. Therefore, the total number of clock cycles must be equal to (16 x *N*), where *N* is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{CS}$ should be taken high. This action prevents any further data from being clocked into the input shift register. The contents in the shift registers are transferred into the relevant input registers on the rising edge of the $\overline{CS}$ signal.

A continuous SCLK source may be used if $\overline{CS}$ can be held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles can be used and $\overline{CS}$ can be taken high some time later. When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC registers, and all analog outputs update simultaneously.

DOUBLE-BUFFERED INTERFACE

The DAC8881 has a double-buffered interface consisting of two register banks: the input register and the DAC latch. The input register is connected directly to the input shift register and the digital code is transferred to the input register upon completion of a valid write sequence. The DAC latch contains the digital code used by the resistor R-2R ladder. The contents of the DAC latch defines the output from the DAC.

Access to the DAC register is controlled by the $\overline{LDAC}$ pin. When $\overline{LDAC}$ is high, the DAC register is latched and the input register can change state without affecting the contents of the DAC latch. When $\overline{LDAC}$ is low, however, the DAC latch becomes transparent and the contents of the input register is transferred to the DAC register.

Load DAC Pin ($\overline{LDAC}$)

$\overline{LDAC}$ transfers data from the input register to the DAC register (and, therefore, updates the DAC output). The contents of the DAC latch (and the output from DAC) can be changed in two ways, depending on the status of $\overline{LDAC}$.

Synchronous Mode

When $\overline{LDAC}$ is tied low, the DAC register updates as soon as new data are transferred into the input register after the rising edge of $\overline{CS}$.

Asynchronous Mode

When $\overline{LDAC}$ is high, the DAC latch is latched. The DAC latch (and DAC output) is not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low, the DAC register updates with the contents of the input register.

1.8V TO 5.5V LOGIC INTERFACE

All digital input and output pins are compatible with any logic supply voltage between 1.8V and 5.5V. Connect the interface logic supply voltage to the IOV_{DD} pin. Although timing is specified down to 2.7V (see the *Timing Characteristics*), IOV_{DD} can operate as low as 1.8V, but with degraded timing and temperature performance. For the lowest power consumption, logic V_{IH} levels should be as close as possible to IOV_{DD}, and logic V_{IL} levels should be as close as possible to GND. Note that the DAC8881 core internal digital logic operates from the same voltage as the 2.7V to 5.5V AV_{DD} supply, so the DV_{DD} pin must also be connected to the AV_{DD} supply voltage.

APPLICATION INFORMATION

BIPOLAR OPERATION USING THE DAC8881

The DAC8881 is designed for single-supply operation; however, a bipolar output range is also possible using the circuit shown in Figure 72. This circuit gives a bipolar output voltage range of V_{BIP}, where V_{BIP} is represented by Equation 2. Note that for this circuit to work, the DAC8881 must operate in the gain = 1X mode configuration with GAIN = DGND. The output voltage for any input code can be calculated with Figure 72:

$$V_{BIP}(CODE) = \left[1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right] \times \frac{CODE}{65536} - \frac{R_3}{R_1} \times V_{REF} \quad (2)$$

Where:

V_{BIP}(CODE) = bipolar output voltage versus CODE from the OPA211.

CODE = 0 to 65535. This is the digital code loaded to the DAC.

V_{REF} = reference high voltage applied to the DAC8881.

By first choosing a value for resistor R_3, R_1 and R_2 can be determined by Equation 3 and Equation 4, respectively:

$$R_1 = \frac{V_{REF}}{V_{BIP}} \times R_3 \quad (3)$$

$$R_2 = \frac{V_{REF} \times R_3}{V_{BIP} - V_{REF}} \quad (4)$$

Where:

V_{BIP}= peak desired output voltage for bipolar output.

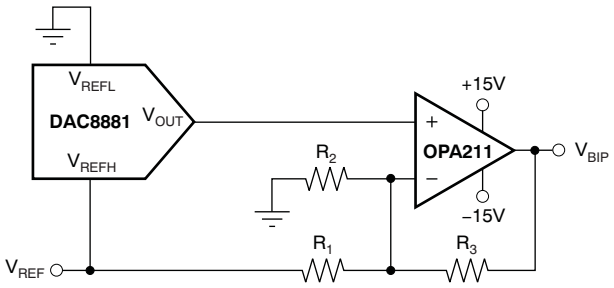
V_{REF} = reference high voltage applied to the DAC8881. NOTE: $V_{BIP} \geq V_{REF}$.

R_3 = OPA211 feedback resistor chosen by user.

Note that R_2 is not required in the circuit of Figure 72 for bipolar output voltage ranges equal to $\pm V_{REF}$.

Using the previous equations, and with V_{REF} = 5V and R_3 set to 10kΩ, a ±8V output span can be achieved with R_1 calculated to be 6.25kΩ and R_2 to be 16.67kΩ.

Similarly, a near ±15V rail-to-rail output can be achieved with R_1 calculated to be 3.33kΩ and R_2 calculated to be 5kΩ.



NOTE: Some pins omitted for clarity.

Figure 72. Bipolar Operation Using the DAC8881

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8881SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8881SRGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8881SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC8881SRGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

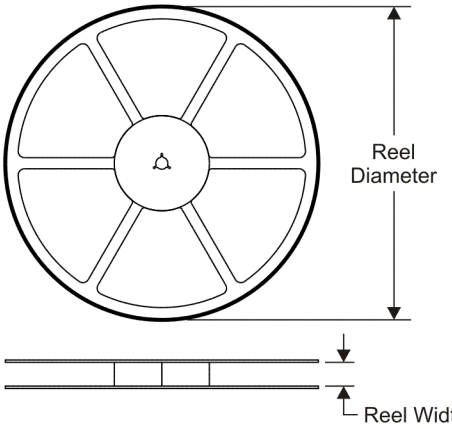
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

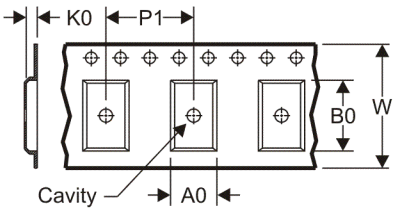
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

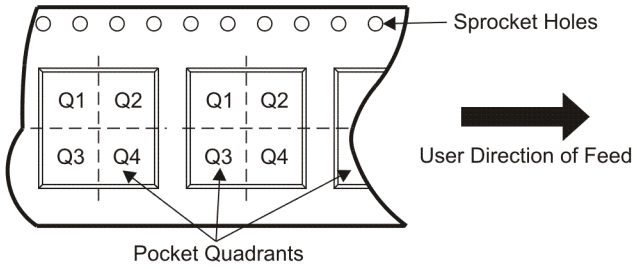


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

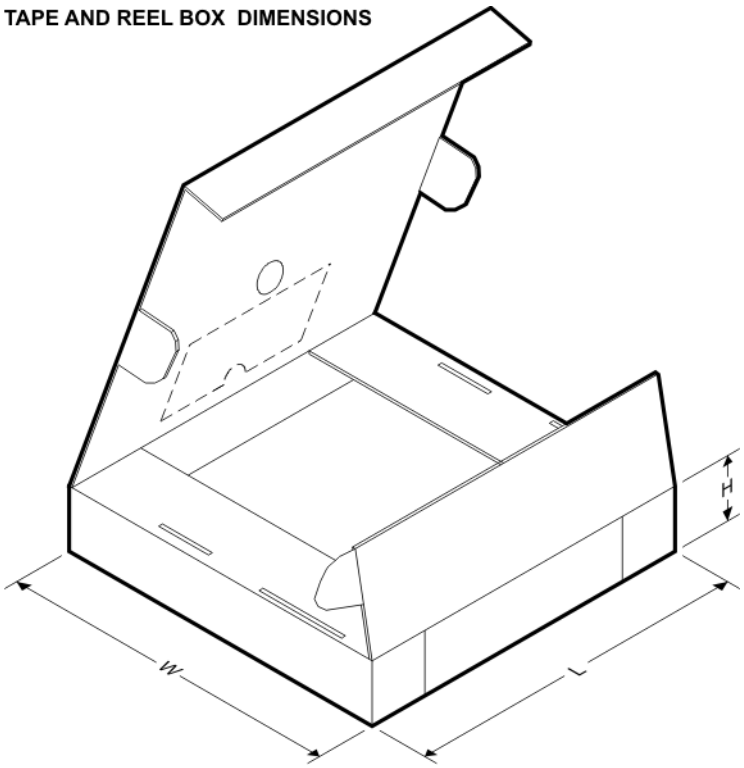
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8881SRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
DAC8881SRGET	VQFN	RGE	24	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

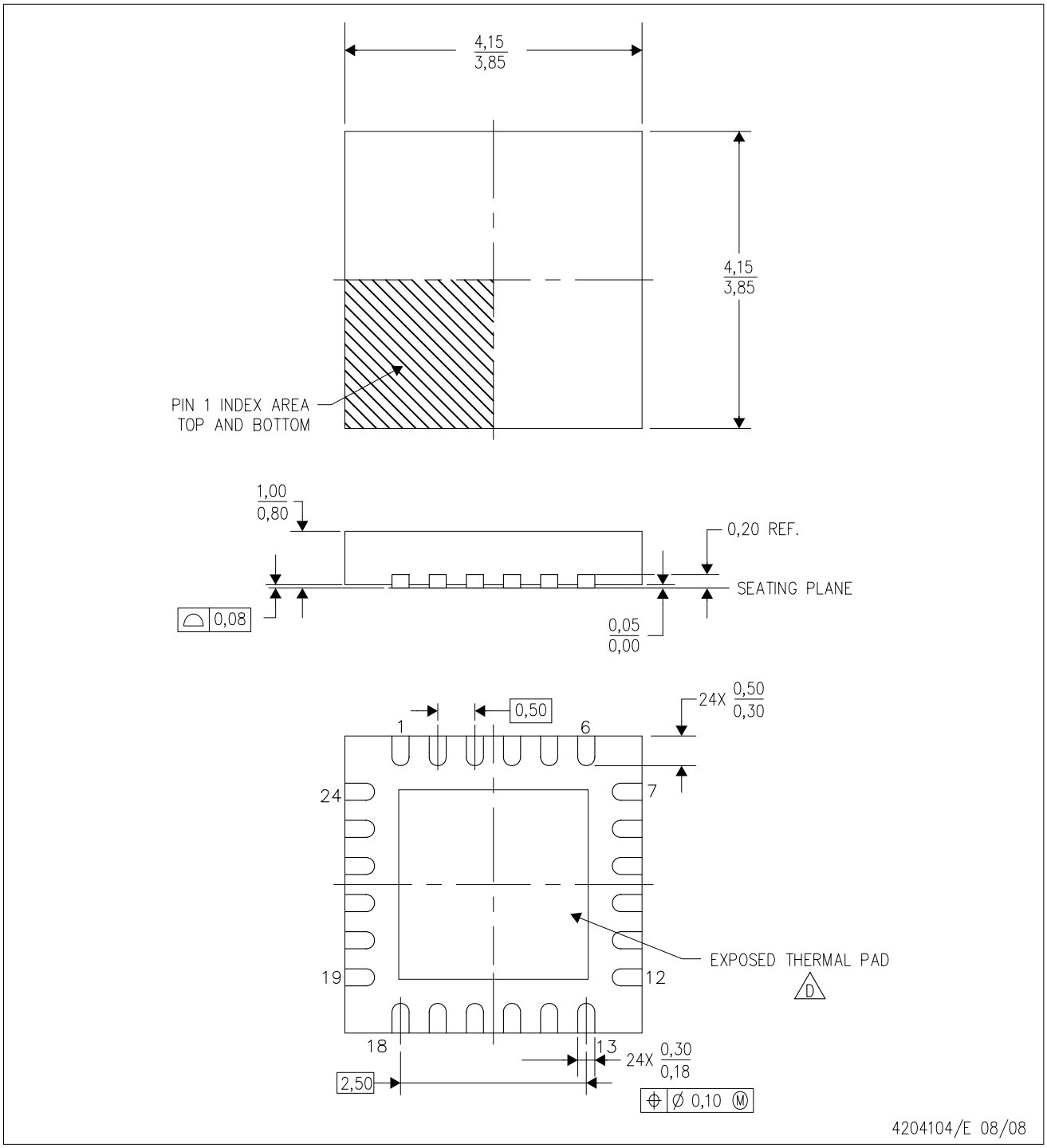
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8881SRGER	VQFN	RGE	24	3000	340.5	333.0	20.6
DAC8881SRGET	VQFN	RGE	24	250	340.5	333.0	20.6

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

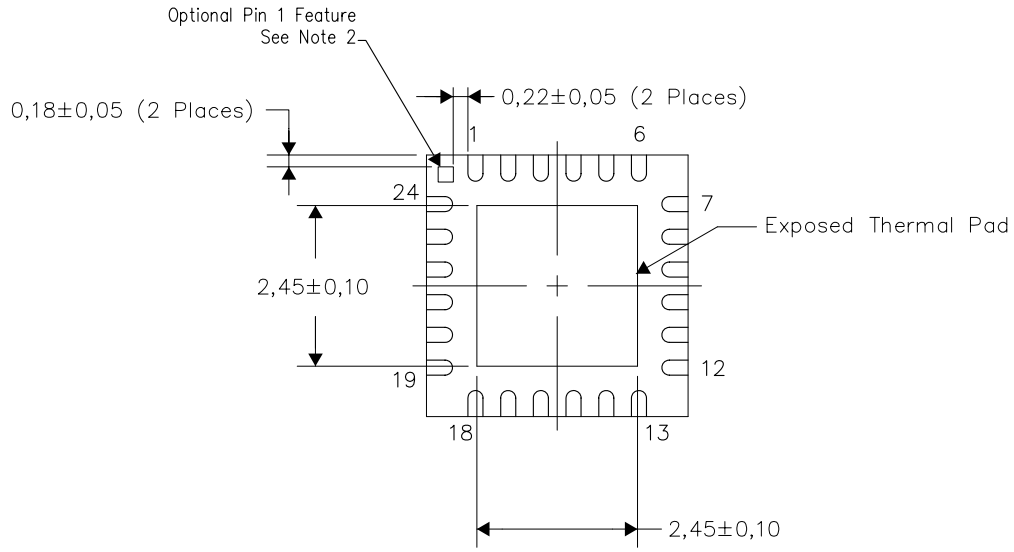
RGE (S–PVQFN–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



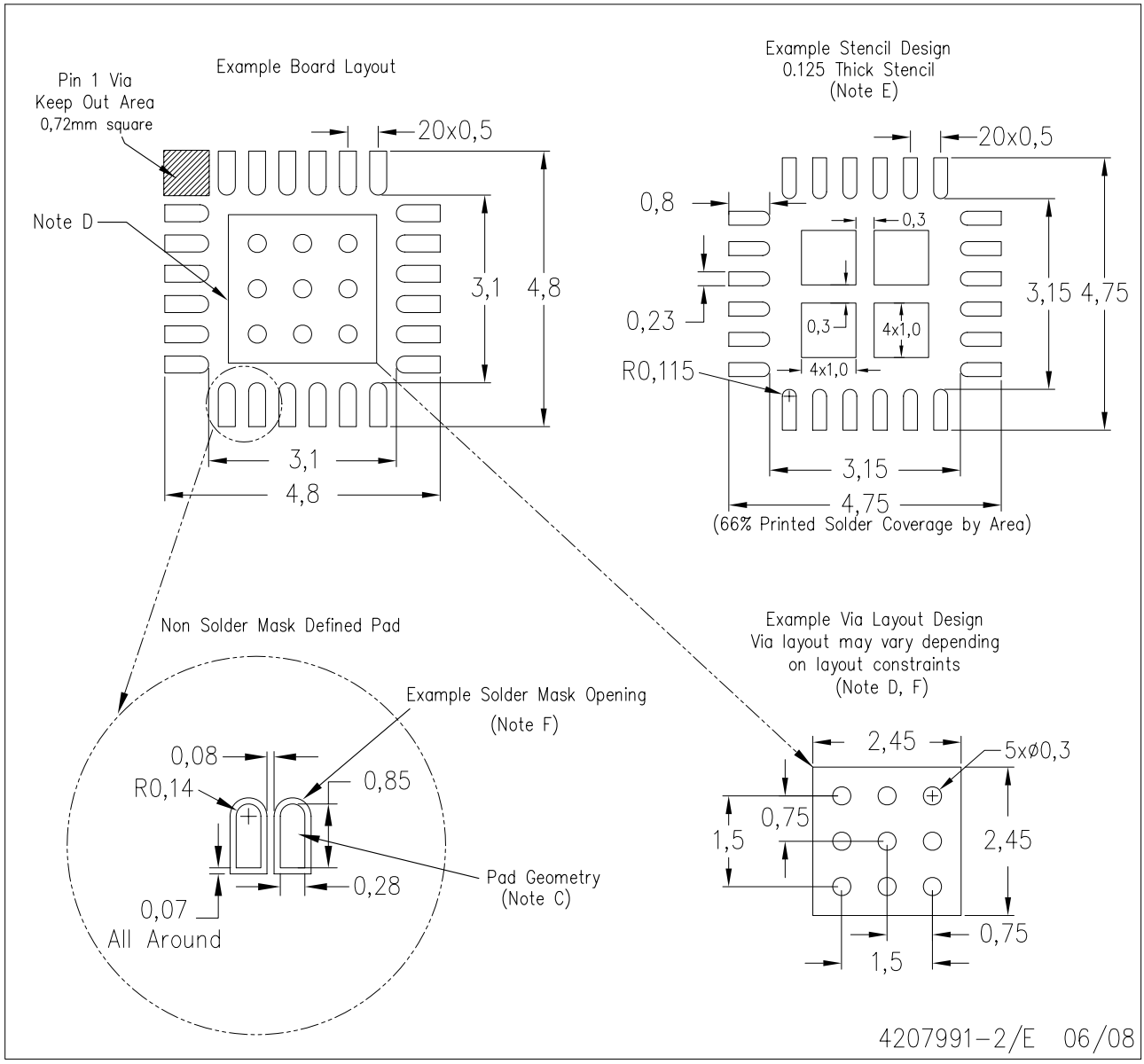
Bottom View

Exposed Thermal Pad Dimensions

NOTES:

1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices
   In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGE (S–PVQFN–N24)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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